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MS-7640^{ATX} Version: 11



CPU:

AMD AM3 (HT 3.0 up to 5.2GT/s)

System Chipset:

North Bridge : ATI RD890
South Bridge : ATI SB850

On Board Chip:

Super I/O : FINTEK F71889ED
LAN : REALTEK RTL8111DL *2
Audio Codec : REALTEK ALC889
IEEE1394 : VIA VT6315N
USB 3.0 : NEC uPD720200 USB
Extend ESATA : JMICRON JMB363
PCIE Switch : PERICOM PI3PCIE2415ZHE
South Bridge : ATI SB850

Main Memory:

Dual Channel DDRIII x 4 (Max 8GB) (800 / 1066 / 1333/ 1600MHz)

Expansion Slots:

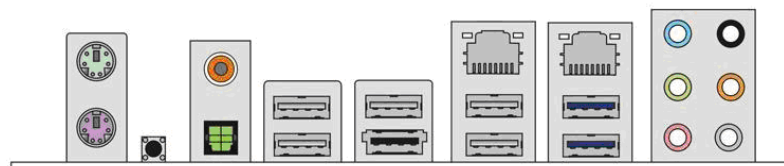
PCI-EPRESS X 16 SLOT x 4
PCI-EPRESS X 4 SLOT x 1
PCI-EPRESS X 1 SLOT x 1
PCI 2.2 SLOT x 1

PWM:

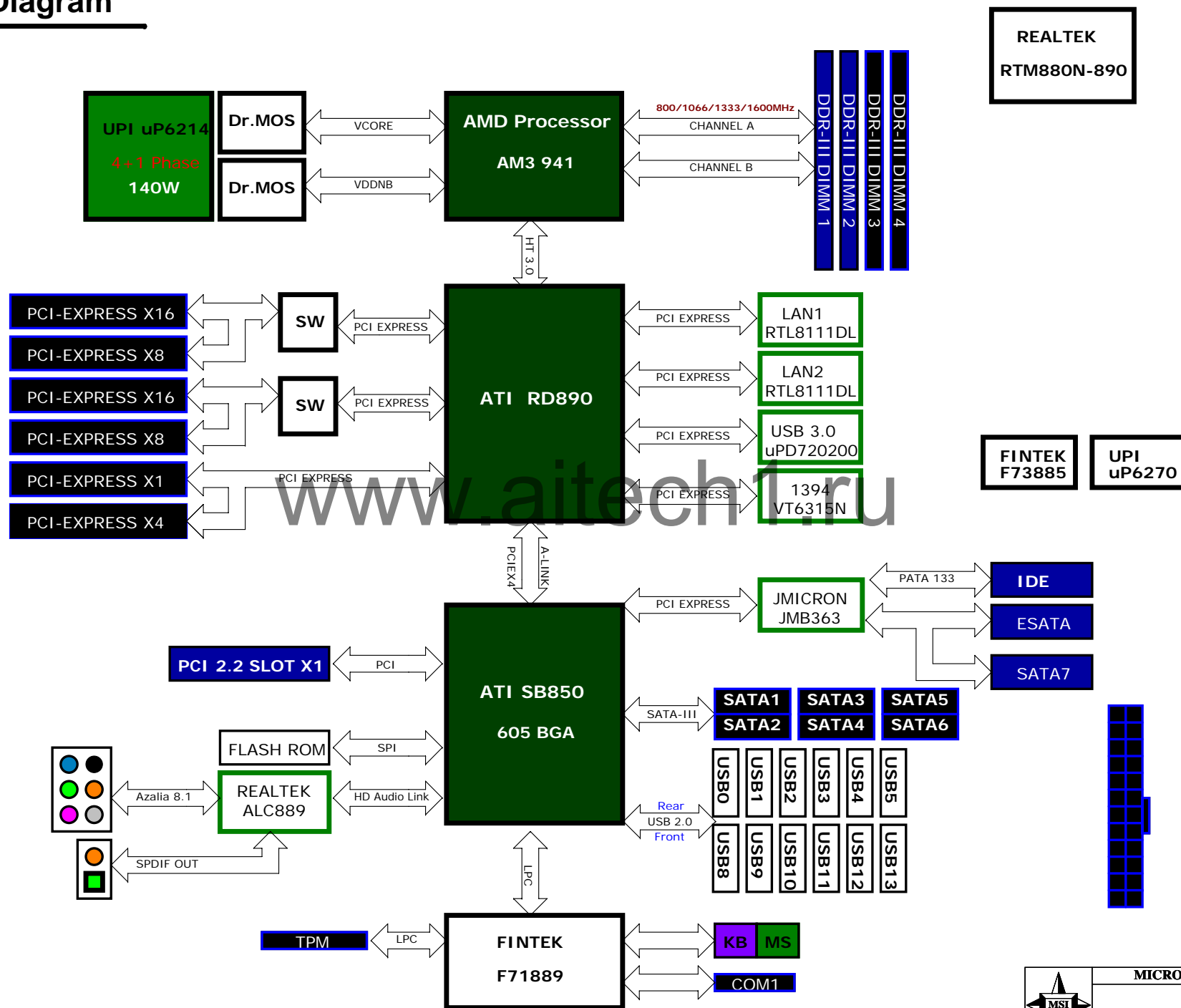
Controller : UPI up6214 + Dr.MOS (4 +1 Phase / 140W)

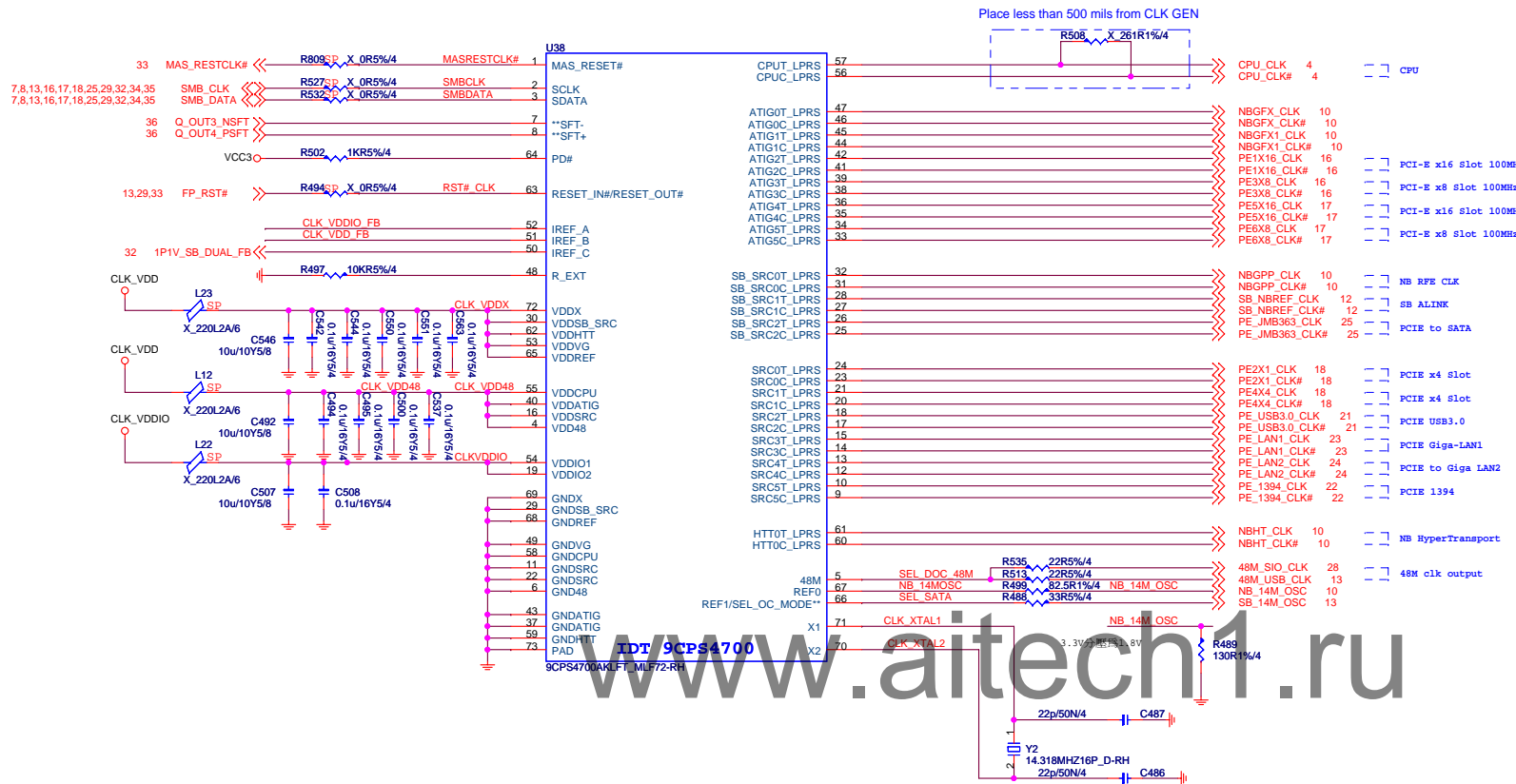
Clock Generator:

Controller : REALTEK RTM880N-890 + ICS9DBL



Block Diagram





for overclocking ability

SEL_SATA 10KR5%/4 R912

CPU CLK C501 X 10P/50N/4

CPU CLK# C502 X 10P/50N/4

48M SIO CLK C543 X 10P/50N/4

48M USB CLK C527 X 10P/50N/4

PE USB3.0 CLK C576 X 4P/50N/4

PE USB3.0 CLK# C568 X 4P/50N/4

PE 1394 CLK C552 X 4P/50N/4

PE 1394 CLK# C548 X 4P/50N/4

PE LAN1 CLK C588 X 4P/50N/4

PE LAN1 CLK# C587 X 4P/50N/4

PE LAN2 CLK C975 X 4P/50N/4

PE LAN2 CLK# C976 X 4P/50N/4

PE JMB363 CLK C445 X 4P/50N/4

PE JMB363 CLK# C446 X 4P/50N/4

PE1X16 CLK C600 X 4P/50N/4

PE1X16 CLK# C599 X 4P/50N/4

PE3X8 CLK C598 X 4P/50N/4

PE3X8 CLK# C597 X 4P/50N/4

PE5X16 CLK C589 X 4P/50N/4

PE5X16 CLK# C572 X 4P/50N/4

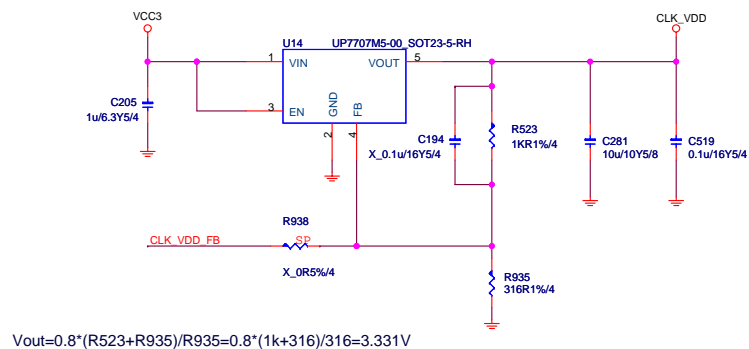
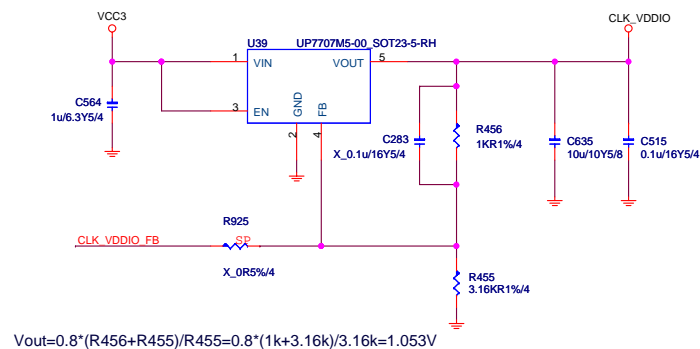
PE6X8 CLK C565 X 4P/50N/4

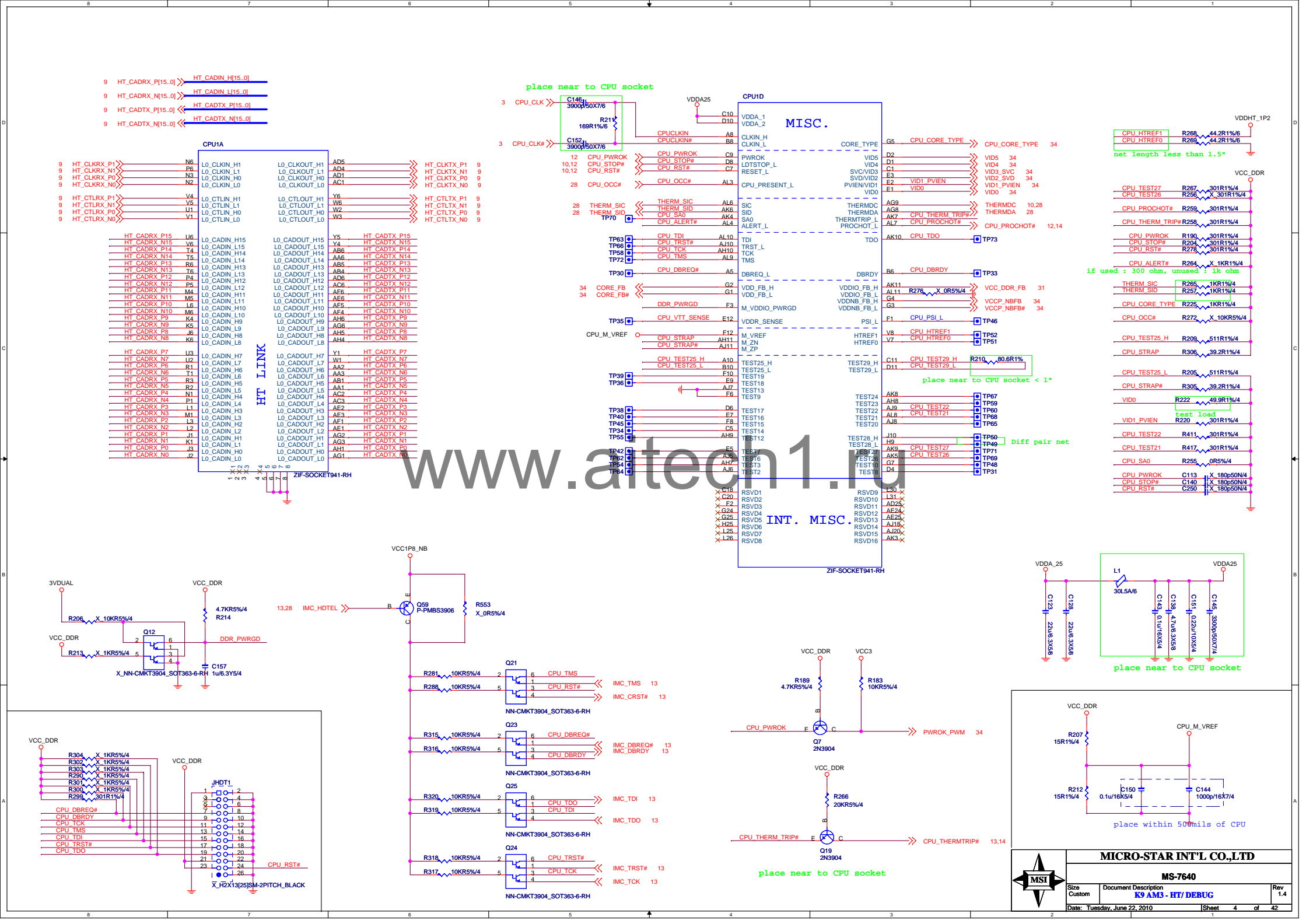
PE6X8 CLK# C559 X 4P/50N/4

PE2X1 CLK# C549 X 4P/50N/4

PE4X4 CLK C619 X 4P/50N/4

PE4X4 CLK# C615 X 4P/50N/4





7 MEM_MA_DQS_N[8..0] <<<<
7 MEM_MA_DQS_P[8..0] <<<<
7 MEM_MA_DATA[63..0] <<<<
7 MEM_MA_DM[7..0] <<<<
7 MEM_MA_ADD[15..0] <<<<
7 MEM_MA_CHECK[7..0] <<<<

AM3

DIMM 4 MB_CLK 5/3 MB1_CLK 1/0
DIMM 3 MB_CLK 2/4 MB0_CLK 1/0
DIMM 2 MA_CLK 5/3 MA1_CLK 1/0
DIMM 1 MA_CLK 2/4 MA0_CLK 1/0

DATA B

DATA A

8 MEM_MB_DM[7..0] <<<<
8 MEM_MB_ADD[15..0] <<<<
8 MEM_MB_CHECK[7..0] <<<<
8 MEM_MB_DATA[63..0] <<<<
8 MEM_MB_DQS_N[8..0] <<<<
8 MEM_MB_DQS_P[8..0] <<<<

CPU1B

TP61 AG21 MA_CLK_H7
TP57 AG20 MA_CLK_L7
TP53 AE20 MA_CLK_H6
TP56 AE19 MA_CLK_L6
U26 MA_CLK_H5
V27 MA_CLK_H4
W27 MA_CLK_L4
W26 MA_CLK_L5
W25 MA_CLK_H3
U24 MA_CLK_L3
U24 MA_CLK_H2
V24 MA_CLK_L2
G19 MA_CLK_H1
H19 MA_CLK_L1
G20 MA_CLK_H0
G21 MA_CLK_L0

AC25 MA0_CS_L1
AA24 MA0_CS_L0

AE28 MA0_ODT1
AC28 MA0_ODT0

AD27 MA1_CS_L1
AA25 MA1_CS_L0

AE27 MA1_ODT1
AC27 MA1_ODT0

TP37 E20 MA_RESET_L

AB25 MA_CAS_L
AB27 MA_WE_L
AA26 MA_RAS_L

N25 MA_BANK2
Y27 MA_BANK1
AA27 MA_BANK0

L27 MA_CKE1
M25 MA_CKE0

M27 MA_ADD15
N24 MA_ADD14
AC26 MA_ADD13
N26 MA_ADD12
P25 MA_ADD11
Y25 MA_ADD10
N27 MA_ADD9
R24 MA_ADD8
P27 MA_ADD7
R25 MA_ADD6
R26 MA_ADD5
R27 MA_ADD4
T25 MA_ADD3
U25 MA_ADD2
T27 MA_ADD1
W24 MA_ADD0

AD15 MA_DQS_H7
AE15 MA_DQS_L7
AG18 MA_DQS_H6
AG19 MA_DQS_L6
AG24 MA_DQS_H5
AG25 MA_DQS_L5
AG27 MA_DQS_H4
AG28 MA_DQS_L4
C29 MA_DQS_H3
C29 MA_DQS_L3
C25 MA_DQS_H2
D25 MA_DQS_L2
F19 MA_DQS_H1
F19 MA_DQS_L1
F15 MA_DQS_H0
G15 MA_DQS_L0

AF15 MA_DM7
AF19 MA_DM6
AJ25 MA_DM5
AH29 MA_DM4
E24 MA_DM3
E18 MA_DM2
E18 MA_DM1
H15 MA_DM0

MA_EVENT_L

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MEM CHA

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CPU1C

TP17 AJ19 MB_CLK_H7
TP19 AK19 MB_CLK_L7
TP18 AL19 MB_CLK_H6
TP20 AL18 MB_CLK_L6
U31 MB_CLK_H5
U30 MB_CLK_L5
W29 MB_CLK_H4
W28 MB_CLK_L4
Y31 MB_CLK_H3
Y30 MB_CLK_L3
V31 MB_CLK_H2
V31 MB_CLK_L2
X31 MB_CLK_H1
X31 MB_CLK_L1
C19 MB_CLK_H0
D19 MB_CLK_L0

AE30 MB0_CS_L1
AC31 MB0_CS_L0

AF31 MB0_ODT1
AD29 MB0_ODT0

AE29 MB1_CS_L1
AB31 MB1_CS_L0

AG31 MB1_ODT1
AD31 MB1_ODT0

B19 MB_RESET_L

AC29 MB_CAS_L
AC30 MB_WE_L
AB29 MB_RAS_L

N31 MB_BANK2
AA31 MB_BANK1
AA28 MB_BANK0

M31 MB_CKE1
M29 MB_CKE0

M28 MB_ADD15
N29 MB_ADD14
AE31 MB_ADD13
N30 MB_ADD12
P29 MB_ADD11
P29 MB_ADD10
P31 MB_ADD9
R28 MB_ADD8
R31 MB_ADD7
R30 MB_ADD6
T31 MB_ADD5
T30 MB_ADD4
U29 MB_ADD3
U28 MB_ADD2
AA30 MB_ADD1
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MEM CHB

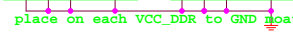
ZIF-SOCKET941-RH



MICRO-STAR INT'L CO.,LTD

MS-7640

Size Custom Document Description K9 AM3 - CPU MEMORY Rev 1.4
Date: Tuesday, June 22, 2010 Sheet 5 of 42

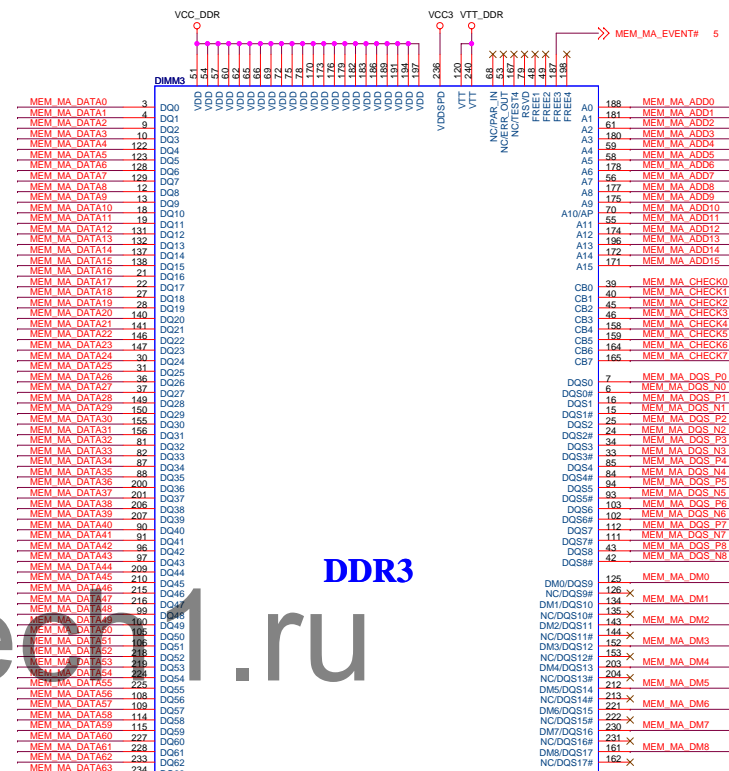
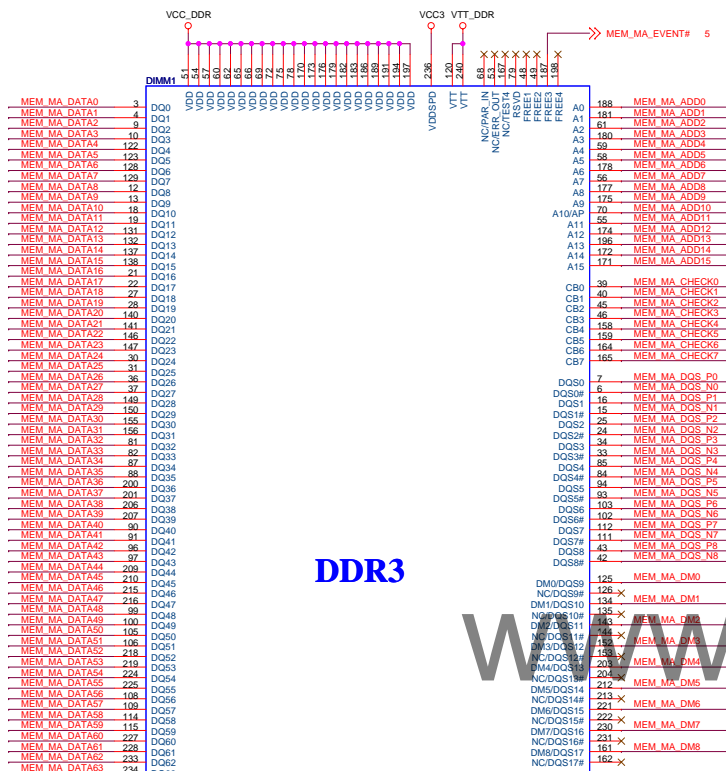


DIMM1 / 0A

DIMM 4	Channel B	ADDR 0B / CNTL 1B / CLK 1B 0/1	0XA6 : 0110
DIMM 3	Channel A	ADDR 0B / CNTL 0B / CLK 0B 0/1	0XA4 : 0100
DIMM 2	Channel B	ADDR 0A / CNTL 1A / CLK 1A 0/1	0XA2 : 0010
DIMM 1	Channel A	ADDR 0A / CNTL 0A / CLK 0A 0/1	0XA0 : 0000

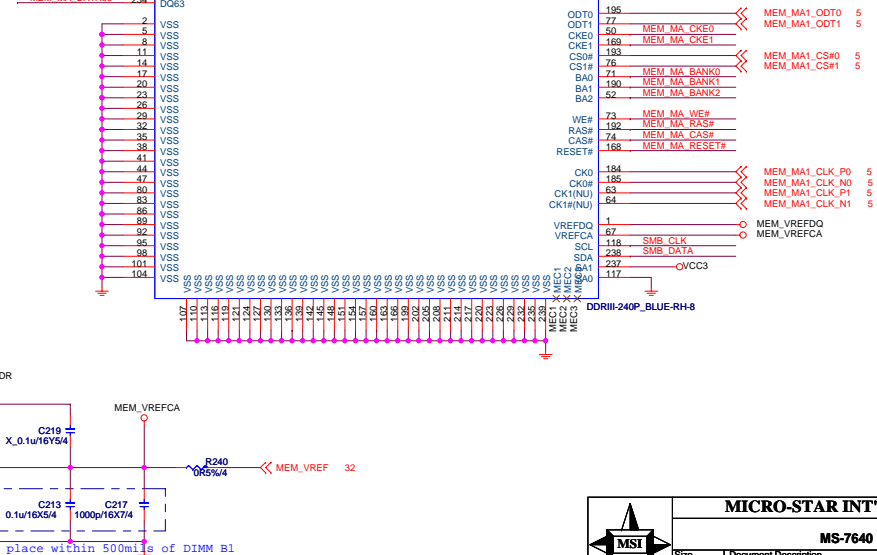
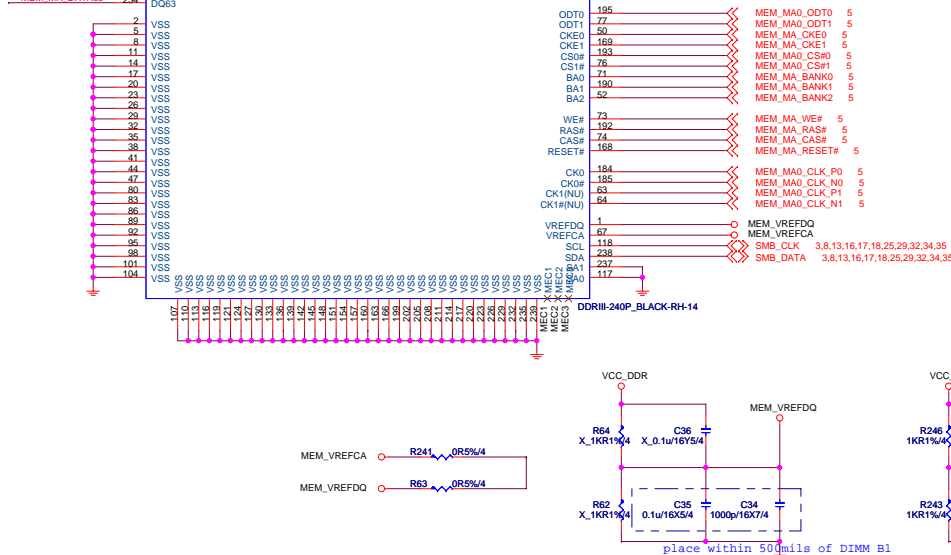
DIMM3 / 1A

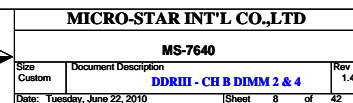
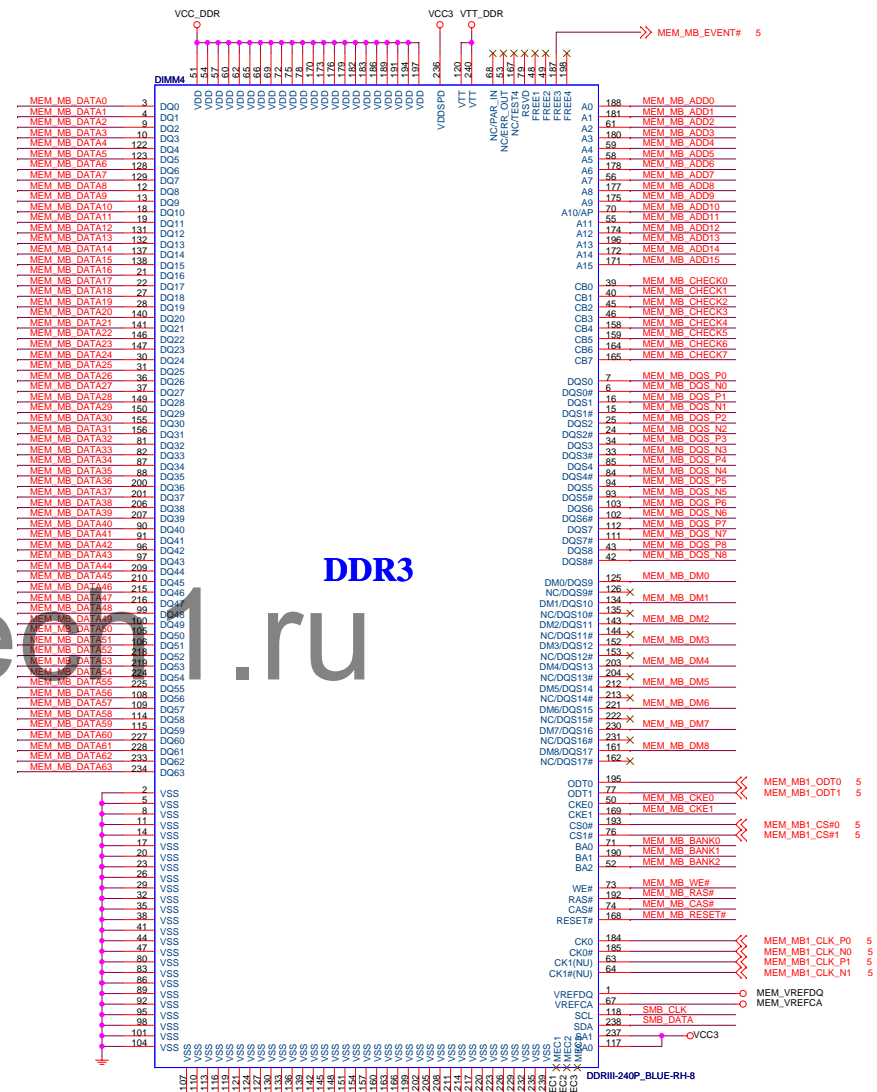
DIMM 2	Channel B	ADDR 0A / CNTL 1A / CLK 1A 0/1	0XA2 : 001
DIMM 1	Channel A	ADDR 0A / CNTL 0A / CLK 0A 0/1	0XA0 : 000

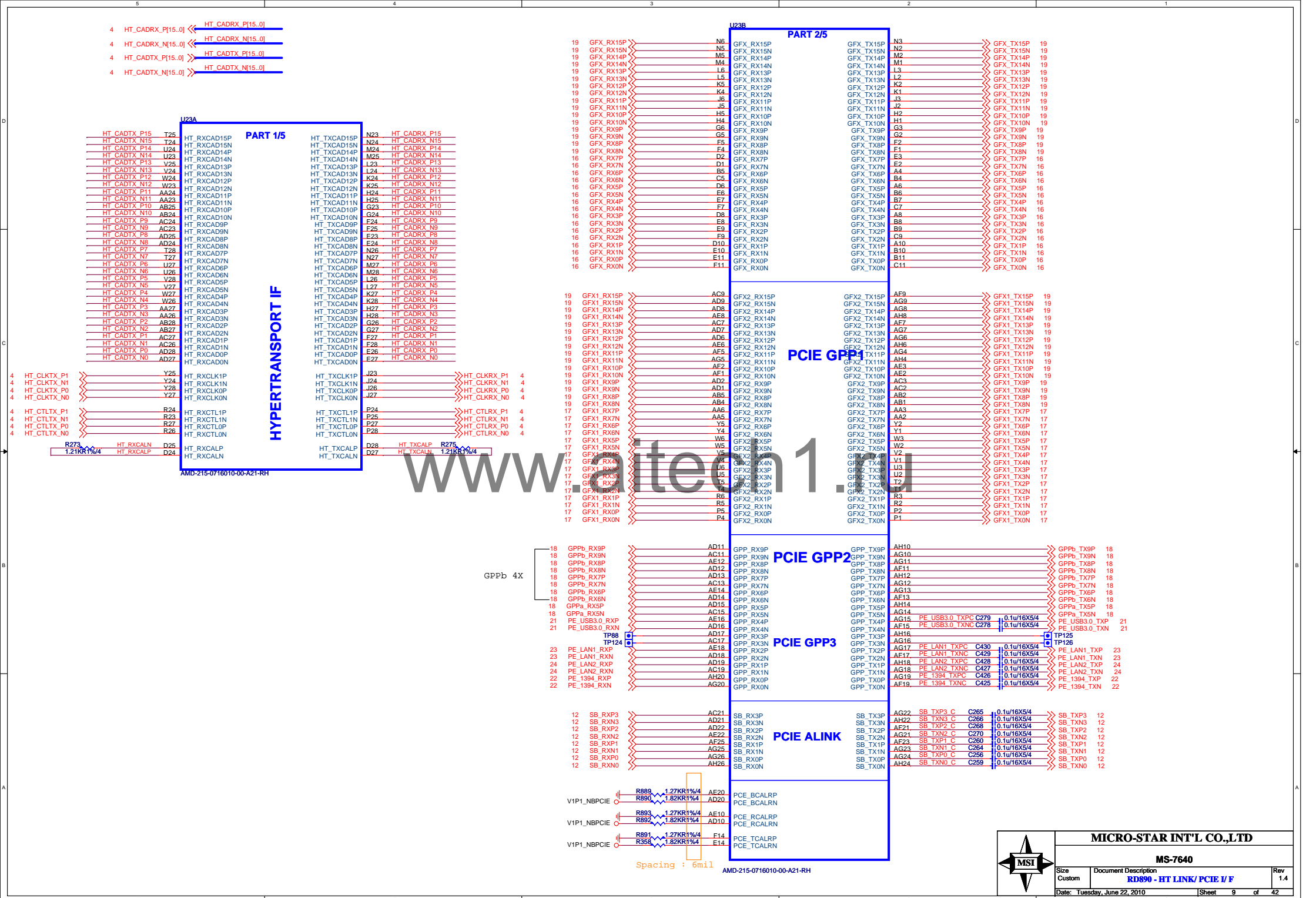


DDR3

DDR3







DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2

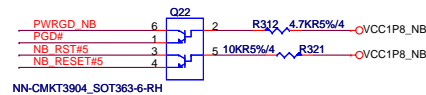
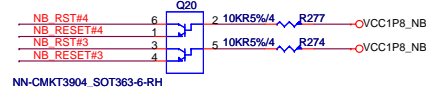
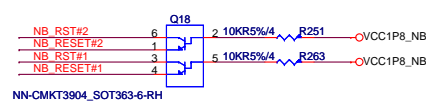
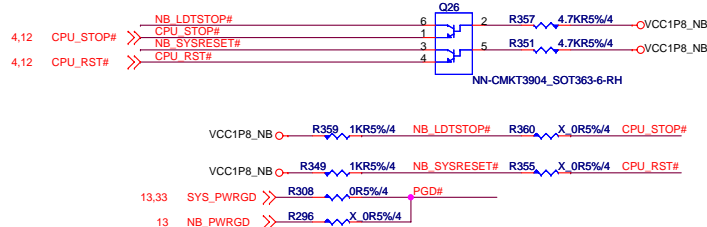
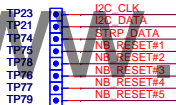
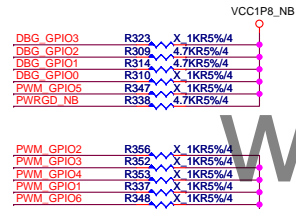
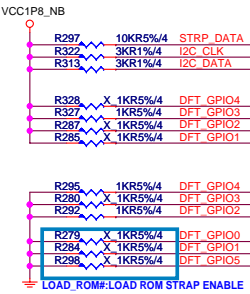
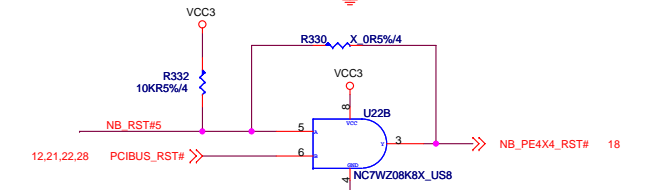
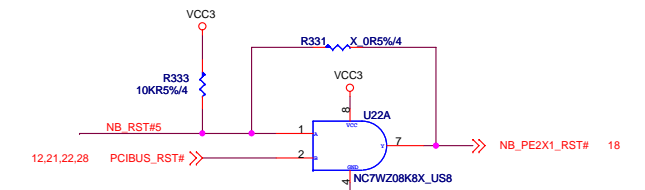
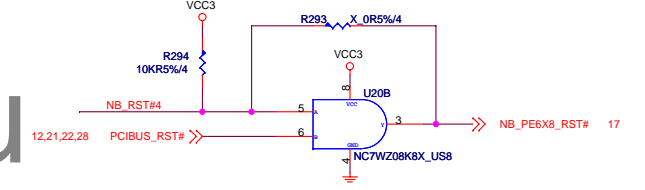
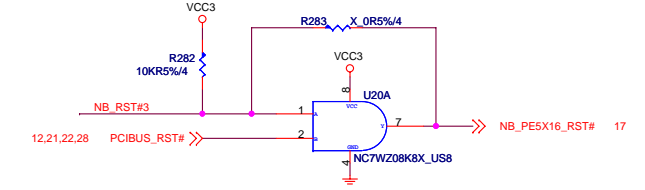
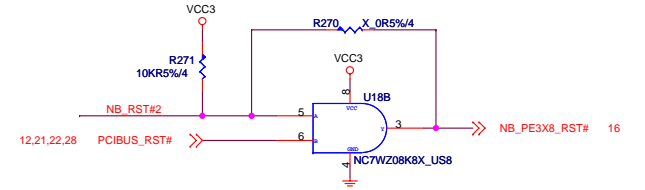
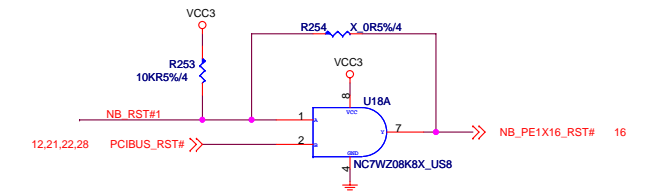
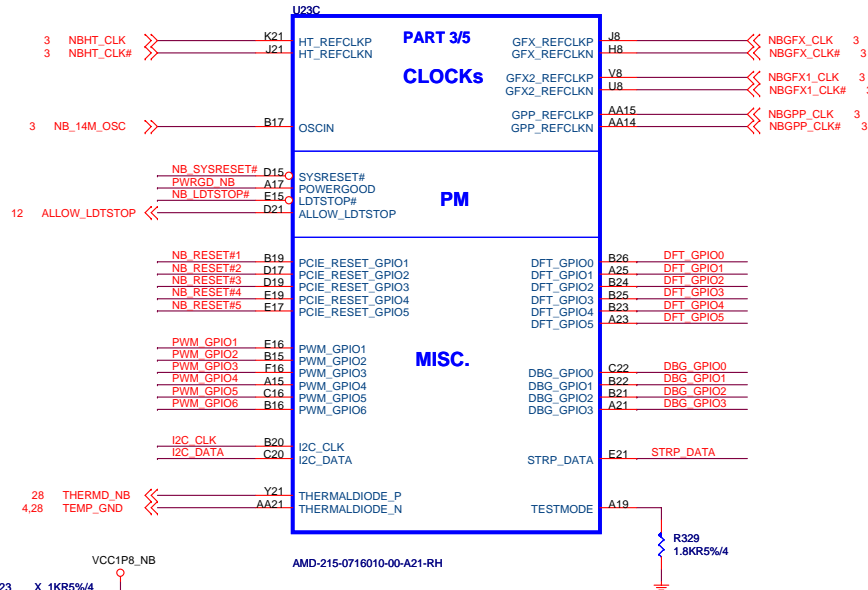
010 : 1:1:1:1:1:4 L

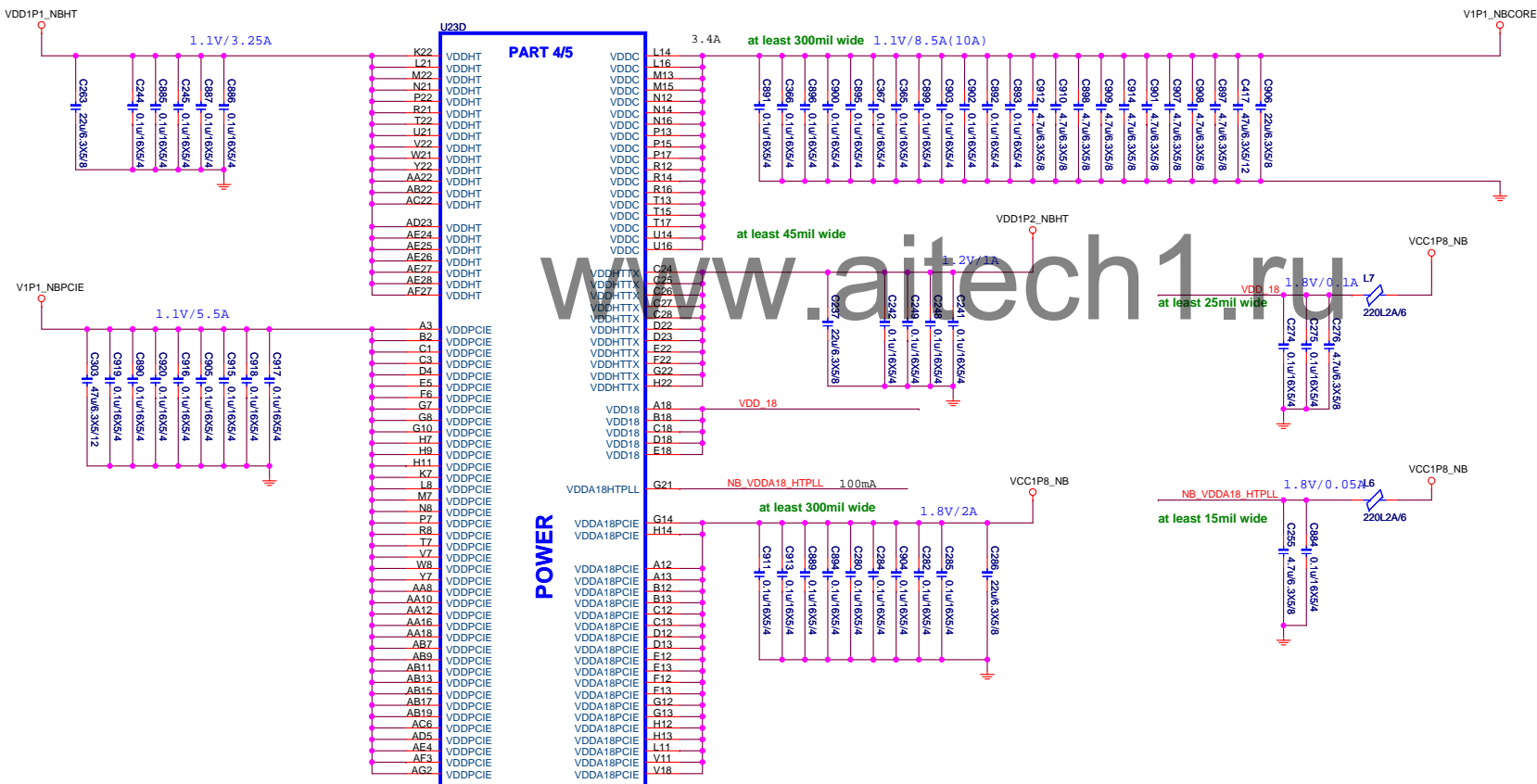
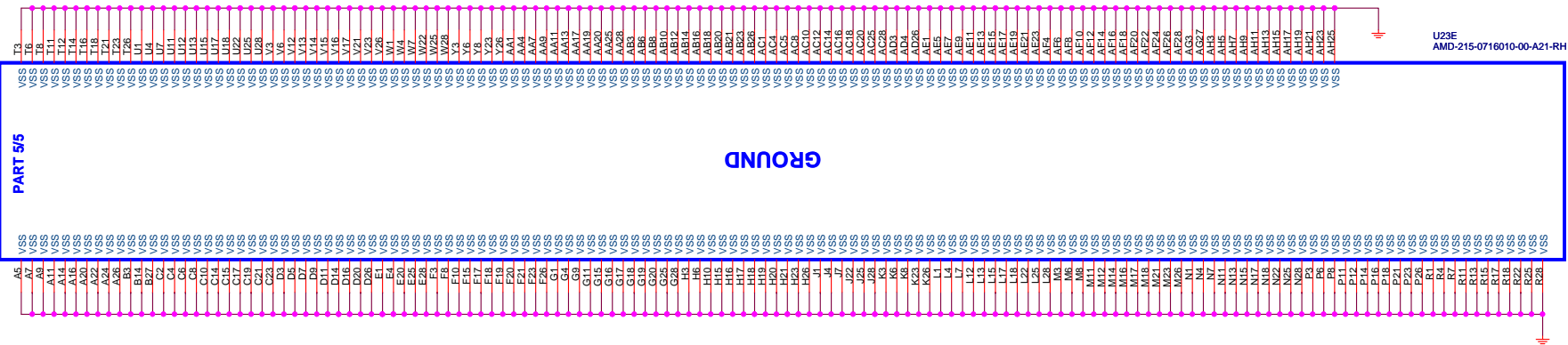
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

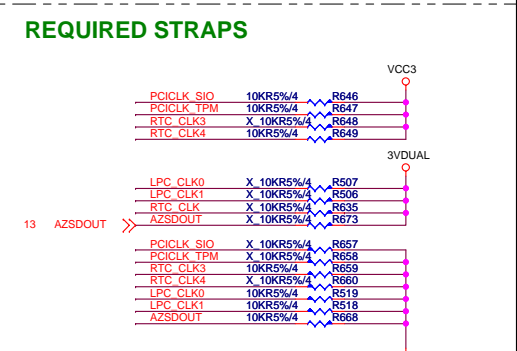
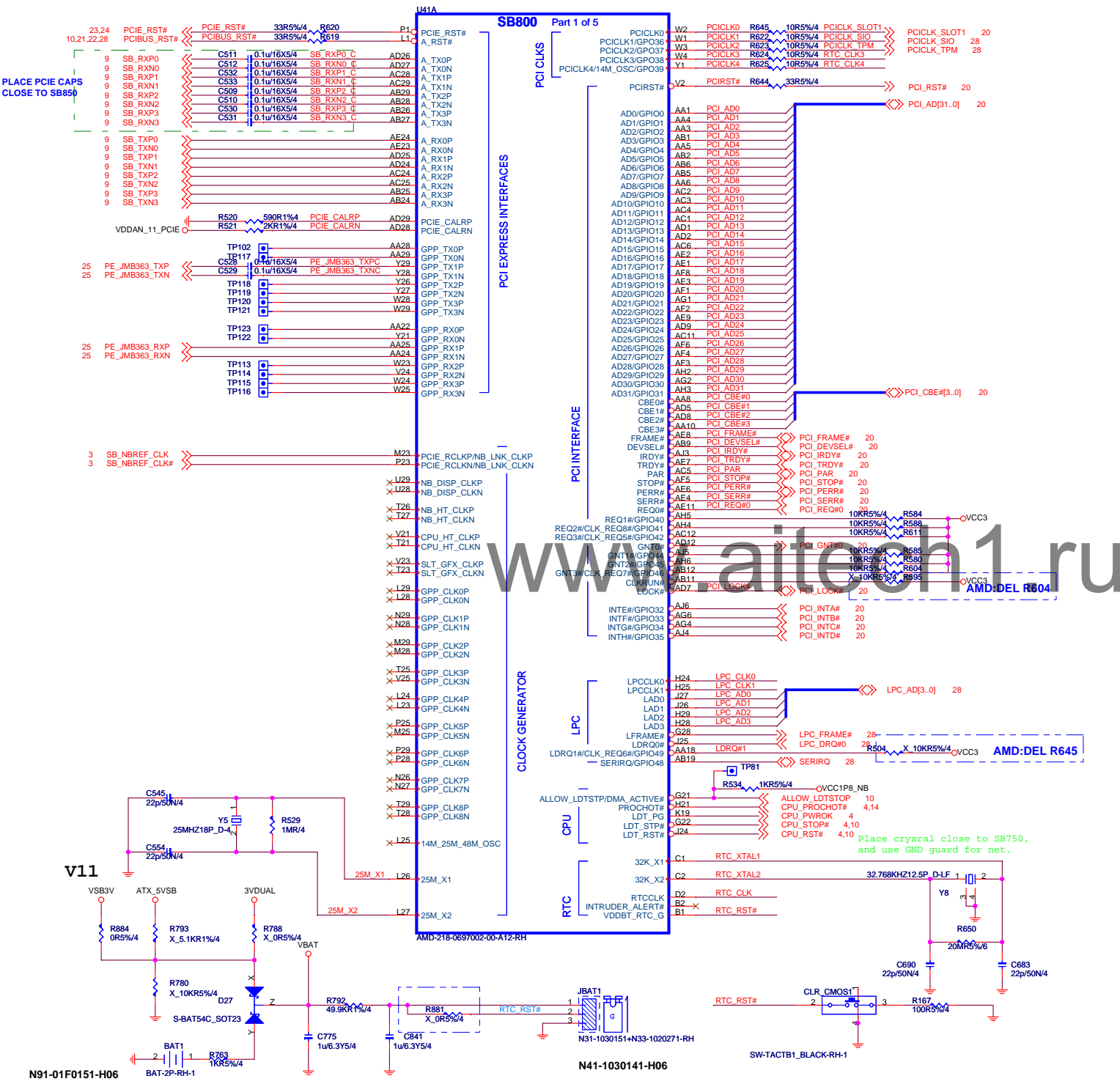
DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLED

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

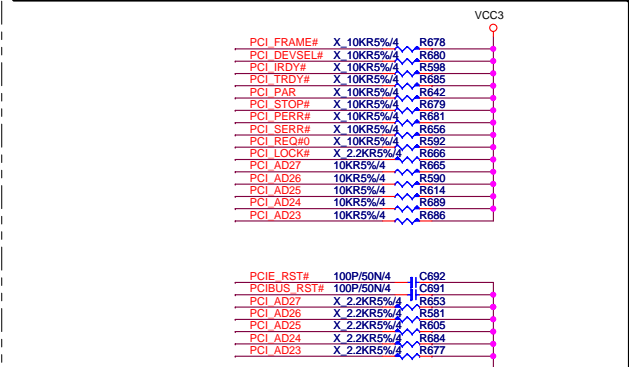





AMD-215-0716010-00-A21-RH



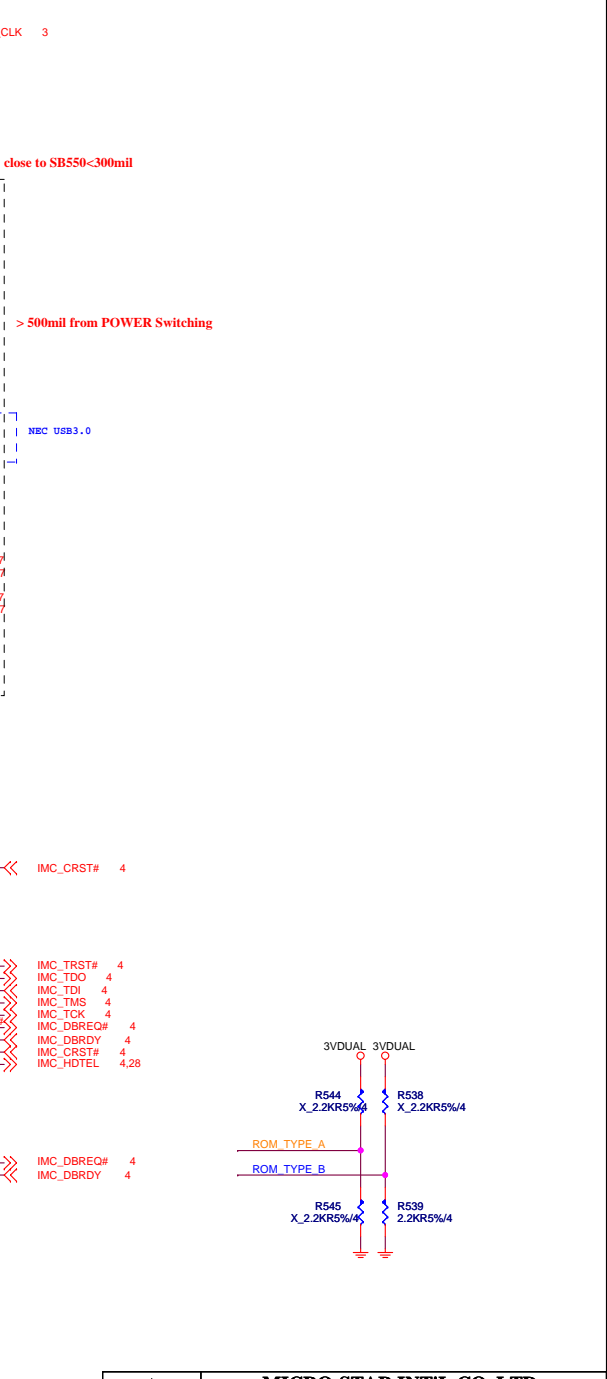
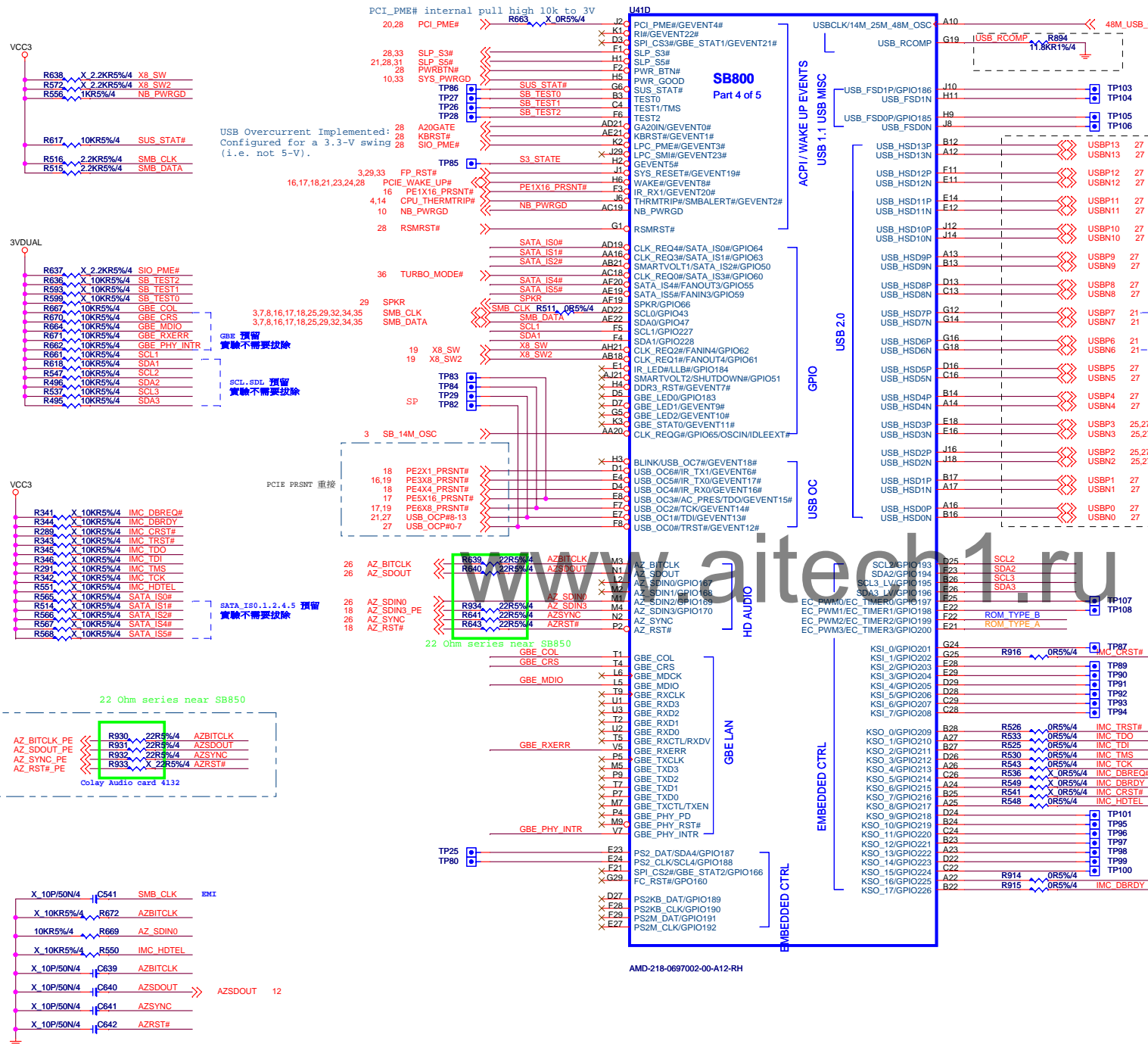
	PULL HIGH	PULL LOW
PCICLK1	Allow PCIe Gen2	Force PCIe Gen 1
PCICLK2	Watchdog timer on NB_PWGRD Enabled	Watchdog timer on NB_PWGRD Disabled
PCICLK3	Denug straps Enabled	Denug straps Disabled
PCICLK4	NON-FUSION CLOCK MODE	FUSION CLOCK MODE
LPC_CLK0	EC ENABLED	EC DISABLED
LPC_CLK1	CLK GEN ENABLE	CLK GEN DISABLE
AZSDOUT	LOW PWR MODE	PERF. MODE



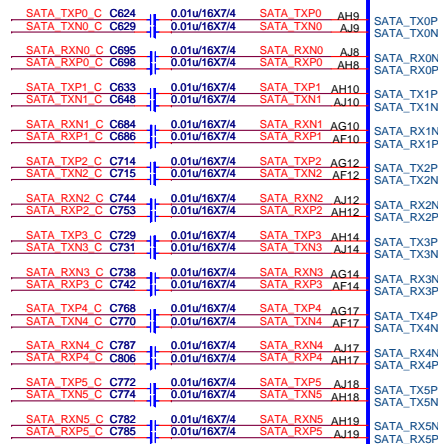
	PULL HIGH	PULL LOW
PCI_AD27	USE PCI PLL	BYPASS PCI PLL
PCI_AD26	DISABLE ILA AUTORUN	ENABLE ILA AUTORUN
PCI_AD25	USE FC PLL	BYPASS FC PLL
PCI_AD24	USE DEFAULT PCIE STRAPS	USE EEPROM PCIE STRAPS
PCI_AD23	DISABLE PCI MEM BOOT	ENABLE PCI MEM BOOT



MICRO-STAR INT'L CO.,LTD
MS-7640
Size Custom Document Description **SB850 - PCIE/PCI/CPU/LPC** Rev 1.4
Date: Tuesday, June 22, 2010 Sheet 12 of 42

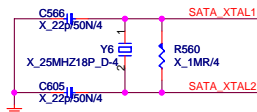


Place AC coupling caps close to
SATA connector
Place AC coupling caps close to SB550 (CRB)

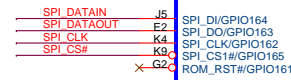


AVDD_SATA 1MR1/4 R896
93R1/4 R895
close SB850 ball
29 SATA_LED# AD11C

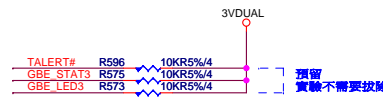
1K 1% for XTAL,
4.99K 1% for 100M INTERNAL CLK



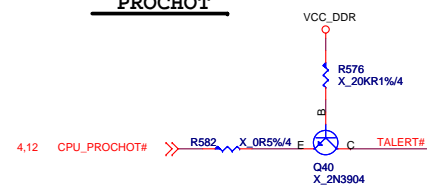
www.aitech.ru



AMD-218-0697002-00-A12-RH

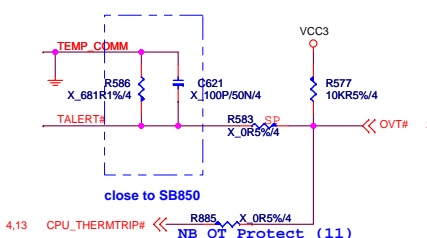


PROCHOT



Temperature Sensing

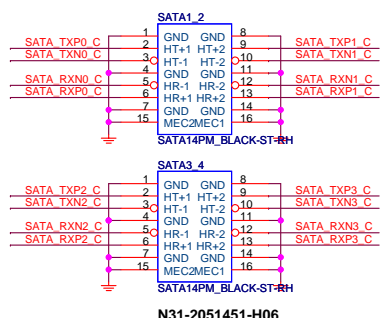
DIODE SENSING CIRCUIT

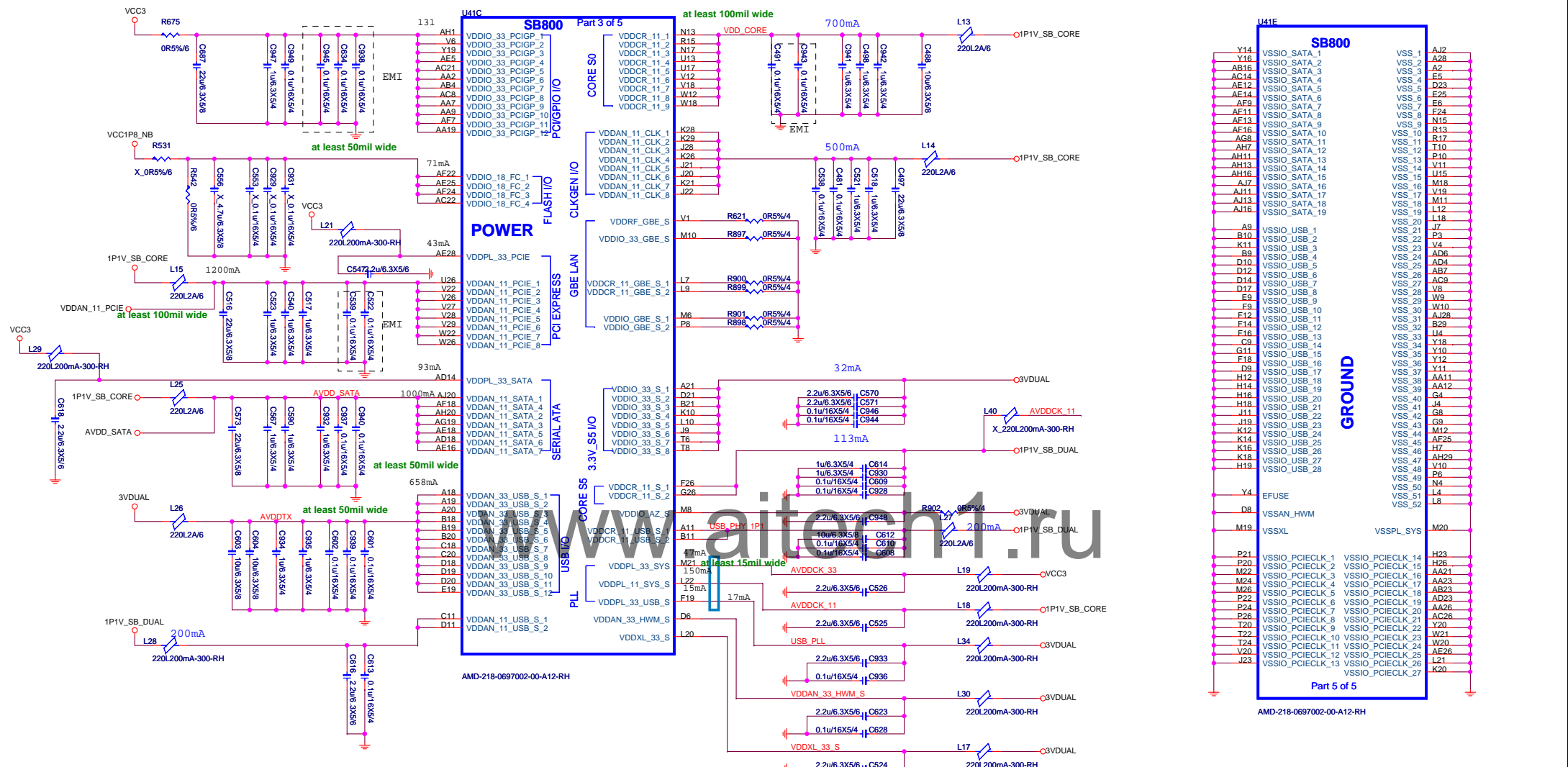


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	SB850 - SATA/ HWM/ SPI	1.4
Date:	Tuesday, June 22, 2010	Sheet 14 of 42





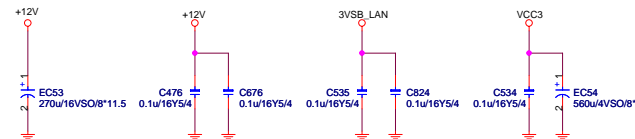
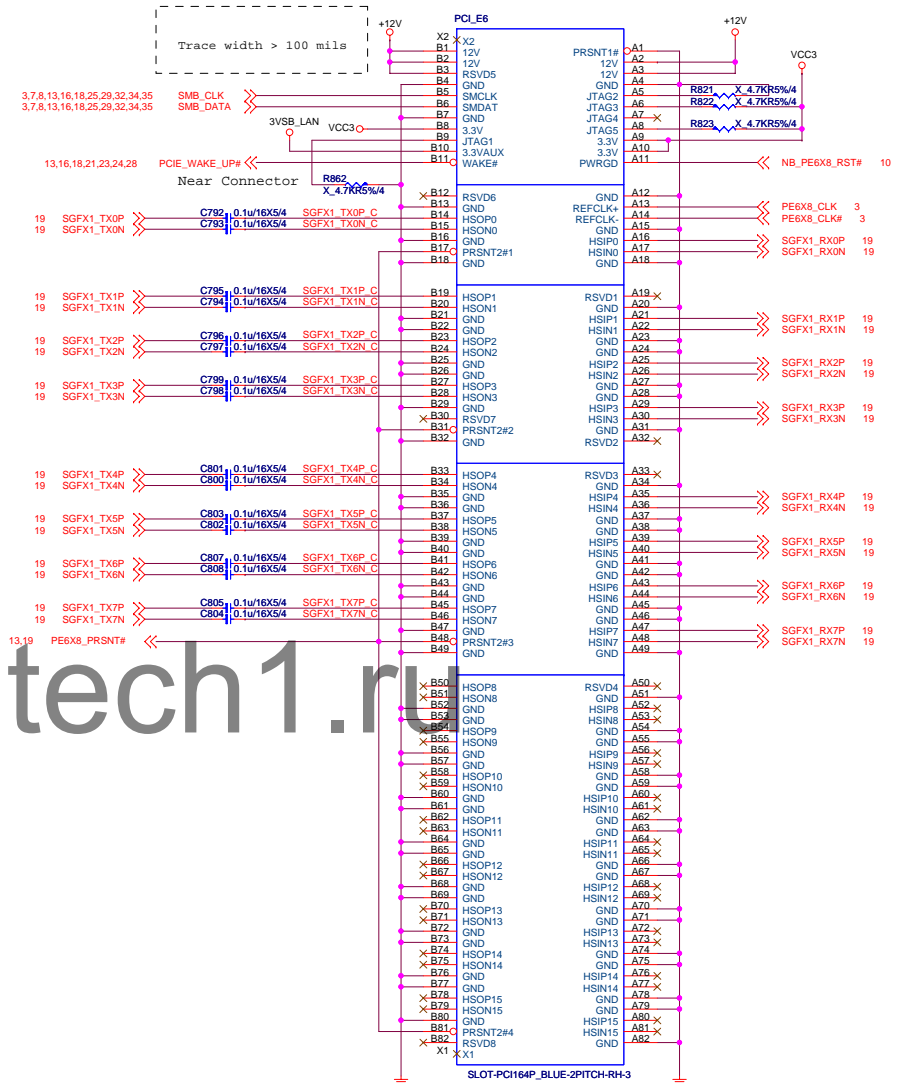
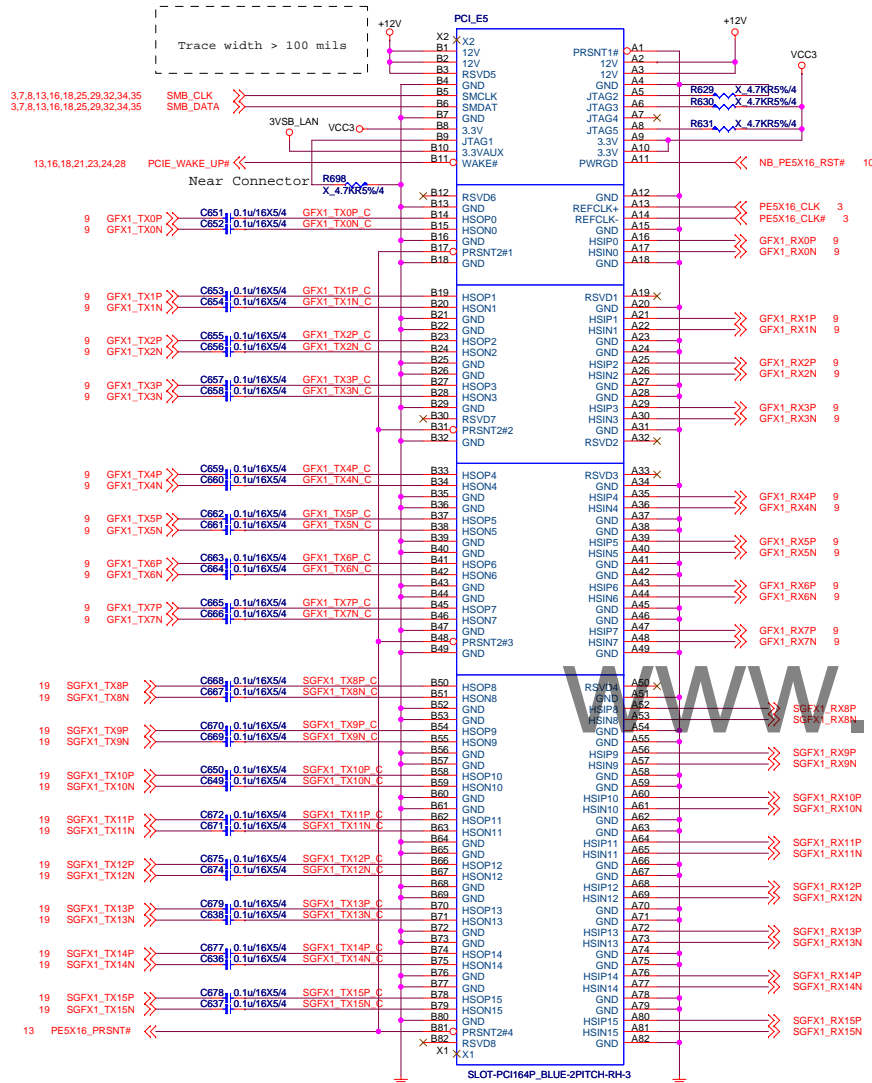
N11-1640711-L06, blue



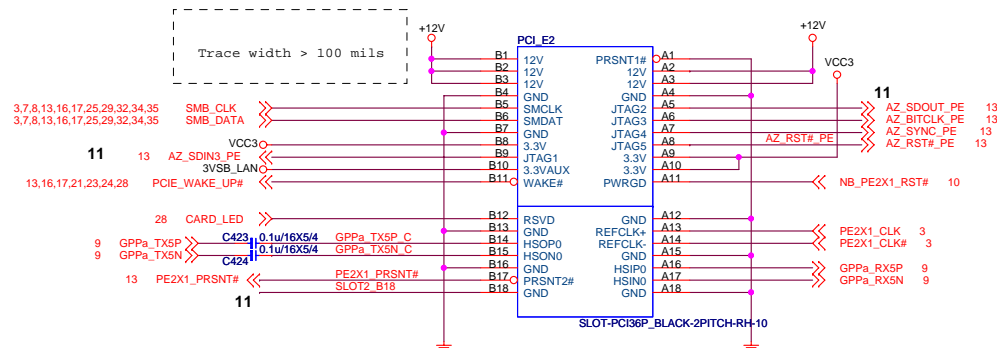
MS-7640

Size Custom	Document Description PCI-Express X16 Slot 1 & 3	Rev 1.4
Date: Tuesday, June 22, 2010		Sheet 16 of 42

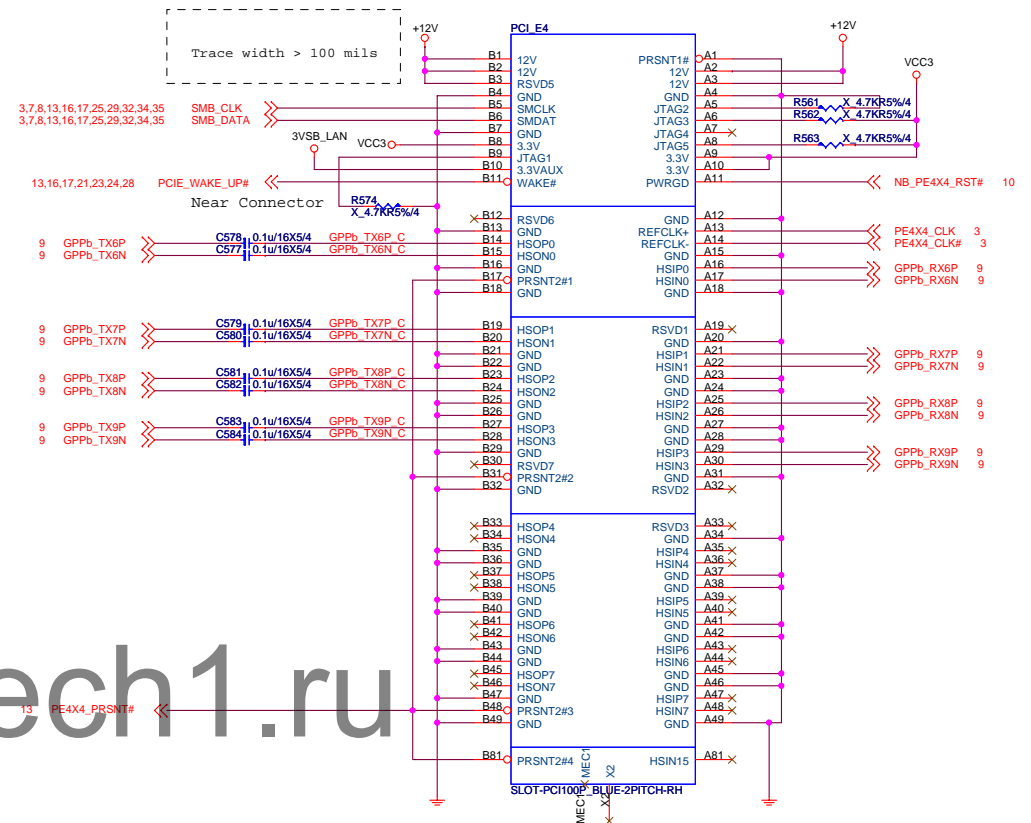
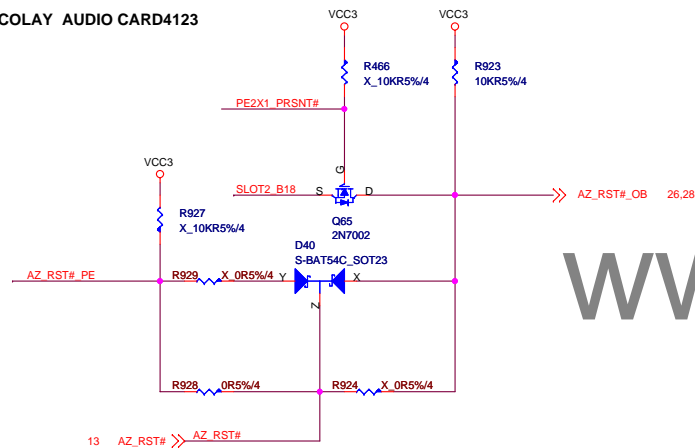
PCI-EXPRESS X16



PCI-EXPRESS X16

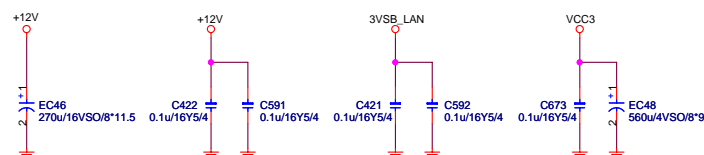


N11-0360281-K06



N11-1000011-L06, Blue (11)

	B17	B18	AZ_RST#_OB	AZ_RST#_PE
N/C	HIGH	N/C	HIGH	HIGH
PEIC X1	GND	GND	HIGH	HIGH
Audio card(4132)	HIGH	GND	LOW	HIGH

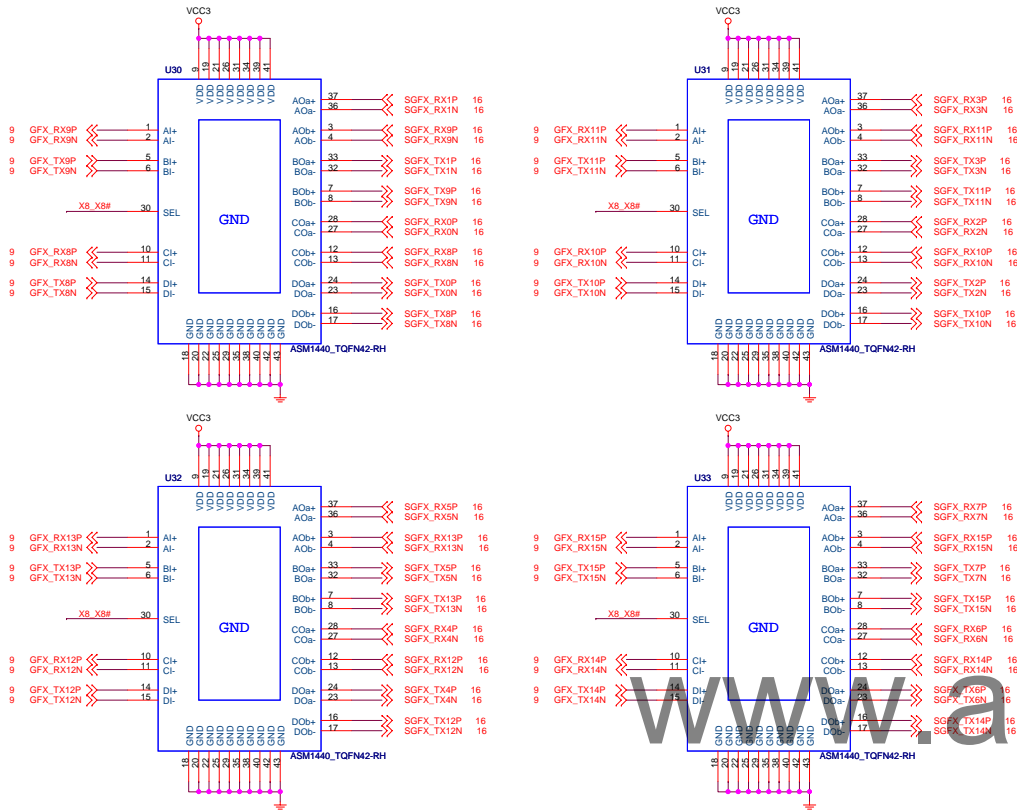


MICRO-STAR INT'L CO.,LTD

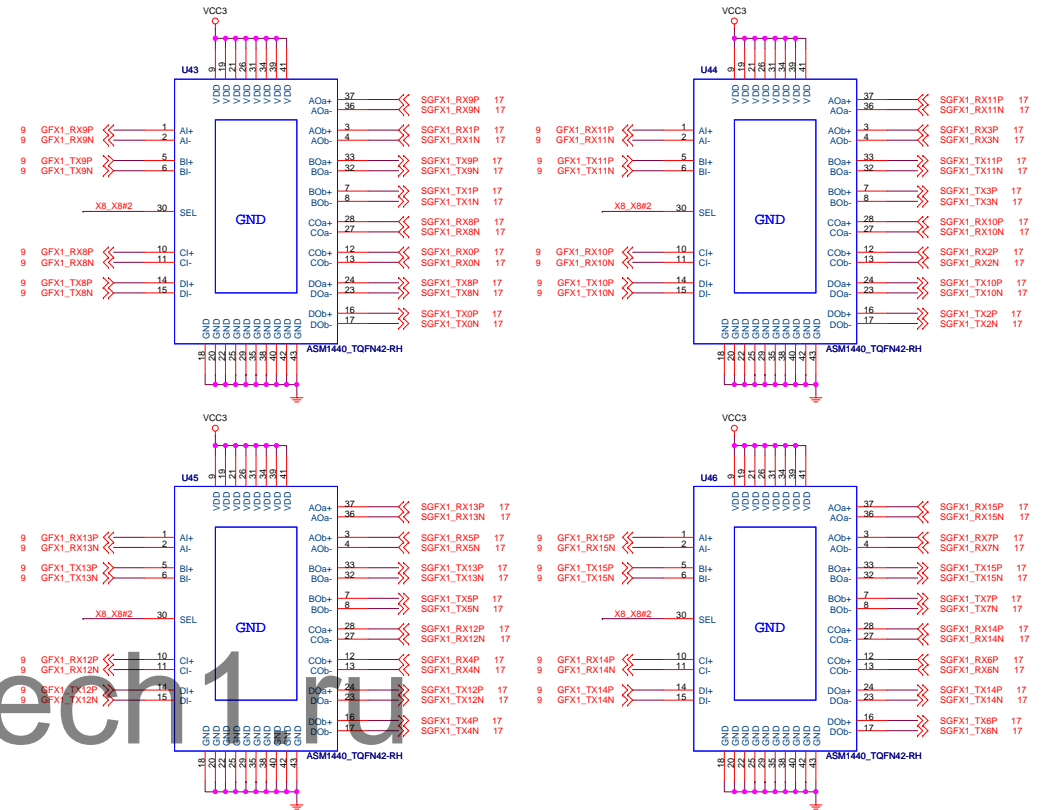
MS-7640

Size Custom	Document Description PCI-Express X4 Slot 2 & 4	Rev 1.4
Date: Tuesday, June 22, 2010		Sheet 18 of 42

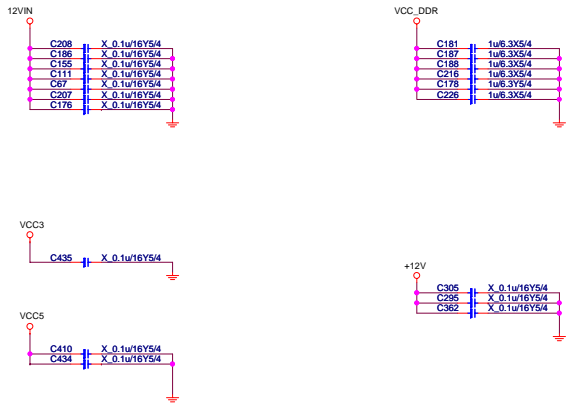
PCI-E SLOT 3 & 6 Switching



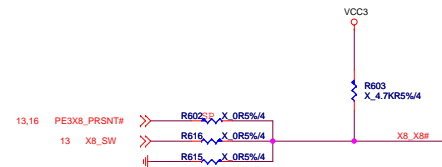
PCI-E SLOT 5 & 6 Switching



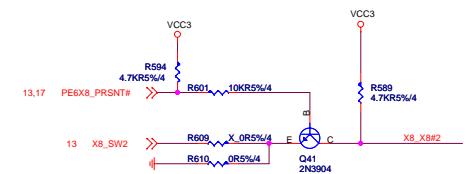
EMI



X8_SW hi for X16



X8_SW low for X16



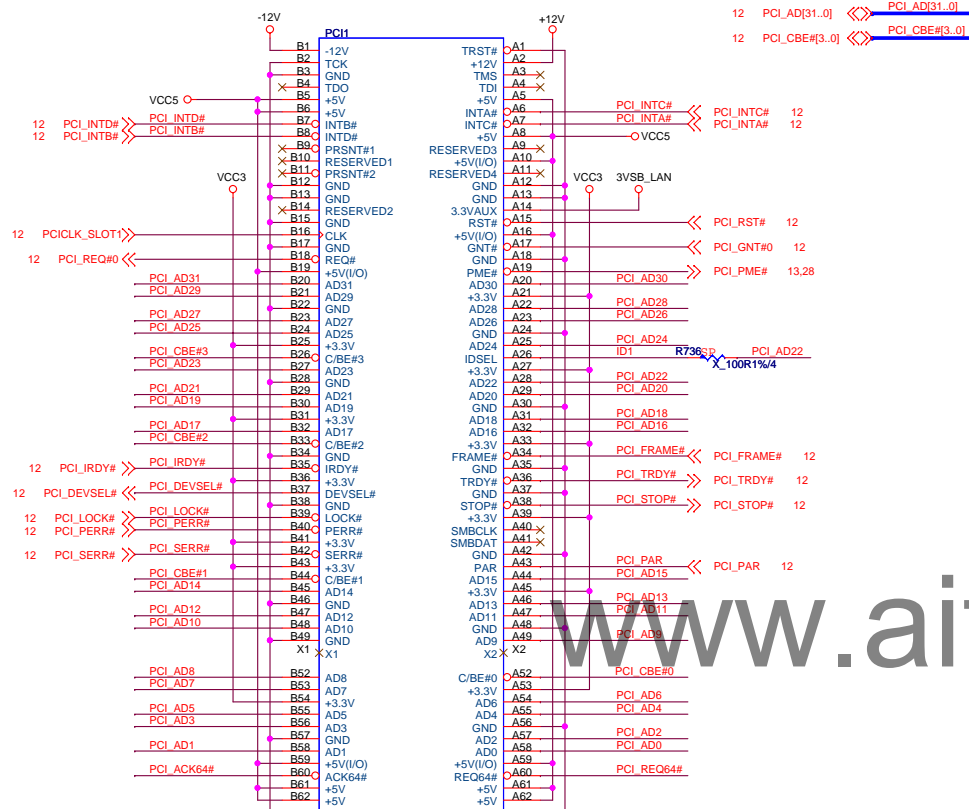
MICRO-STAR INT'L CO., LTD

MS-7640

Size Custom Document Description PCI-Express Slot 2/4 SW Rev 1.4

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PCI SLOT 1 (PCI VER: 2.2 COMPLY)

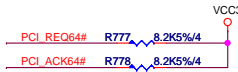


SLOT-PCI_BLACK-1.27PITCH-RH
N11-1200391-F02 (Black)

IDSEL = AD22

MASTER = PCI_REQ#0

PCI_GNT#0



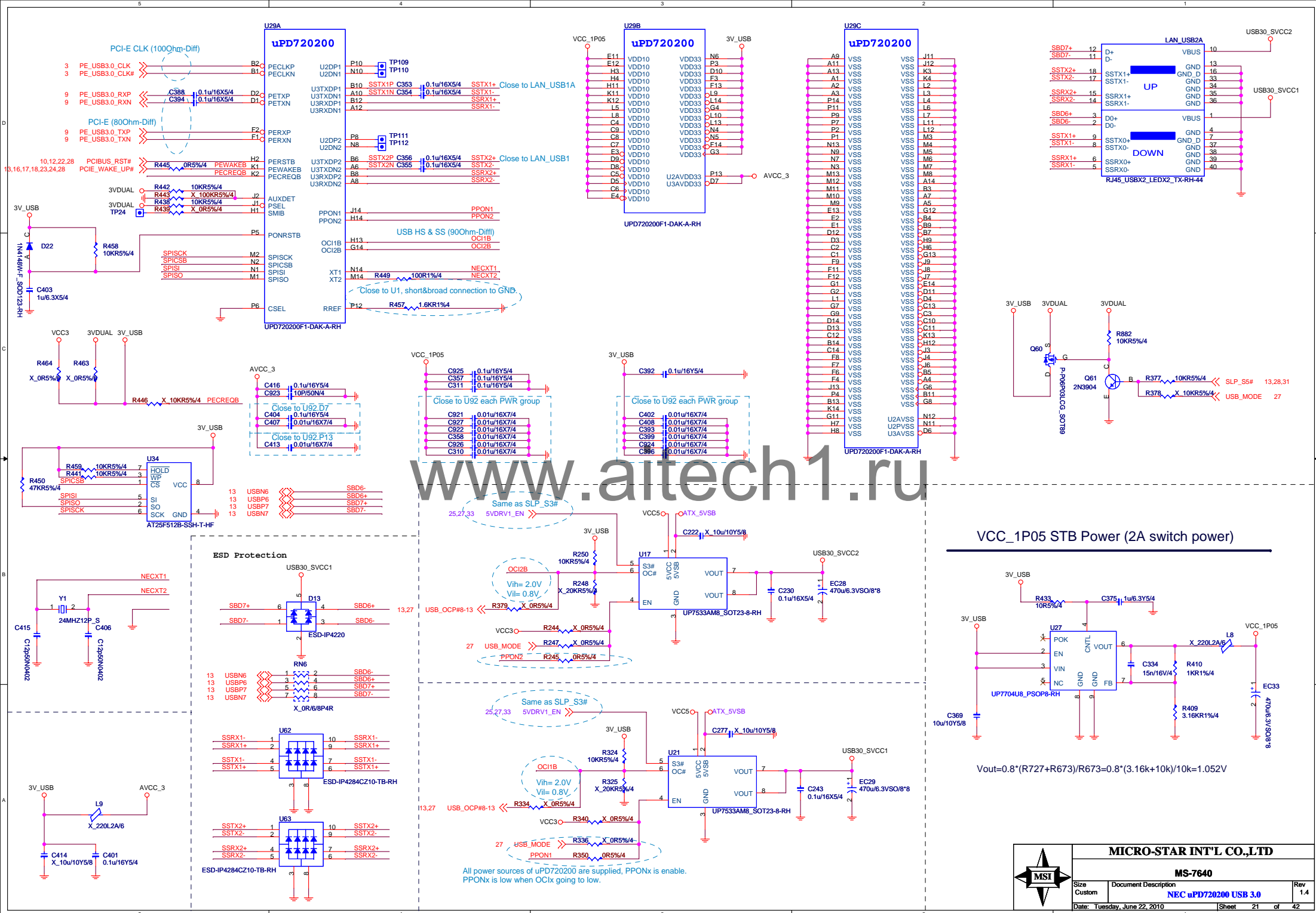
www.aitech1.ru

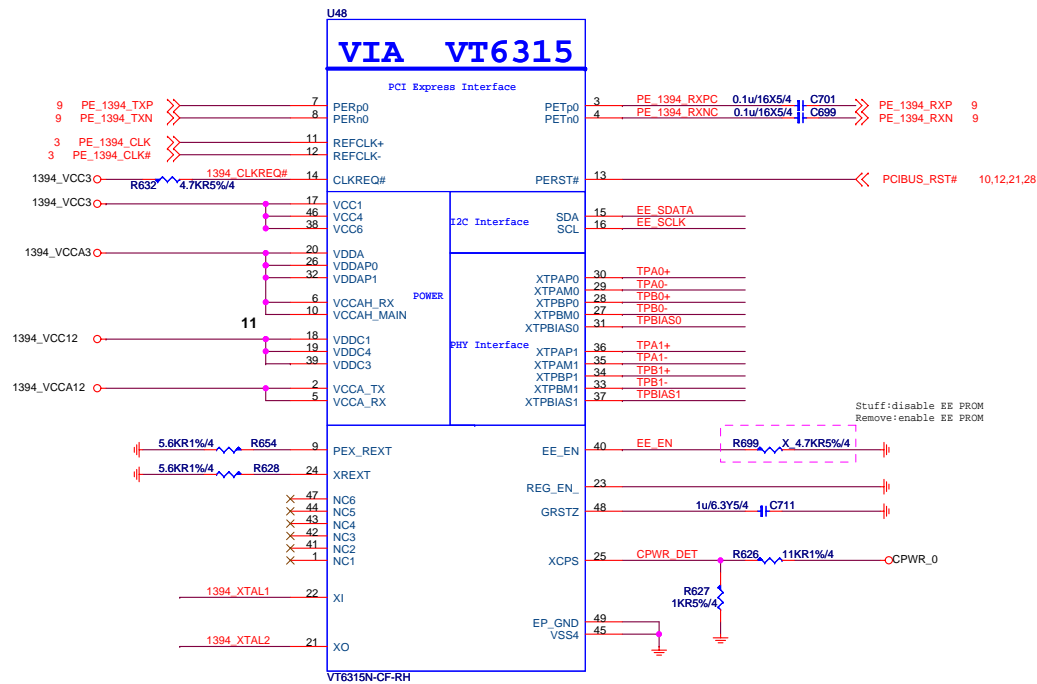


MICRO-STAR INT'L CO.,LTD

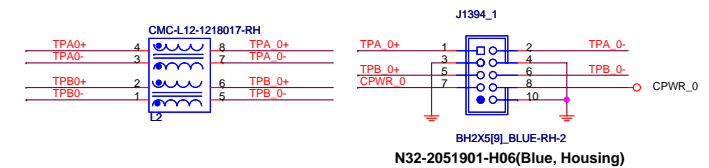
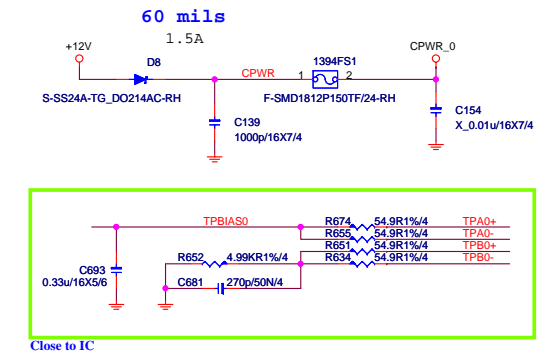
MS-7640

Size	Document Description	Rev
Custom	PCI Slot 1	1.4
Date: Tuesday, June 22, 2010	Sheet 20 of 42	

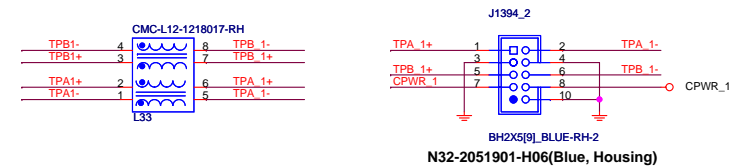
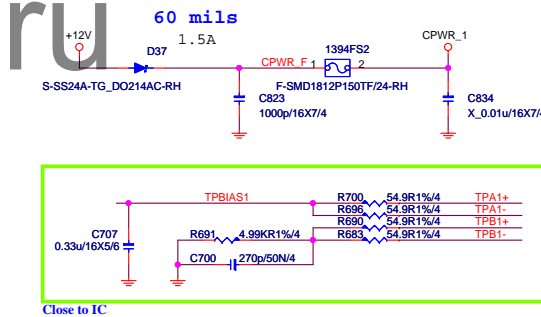




Rear 1394 port

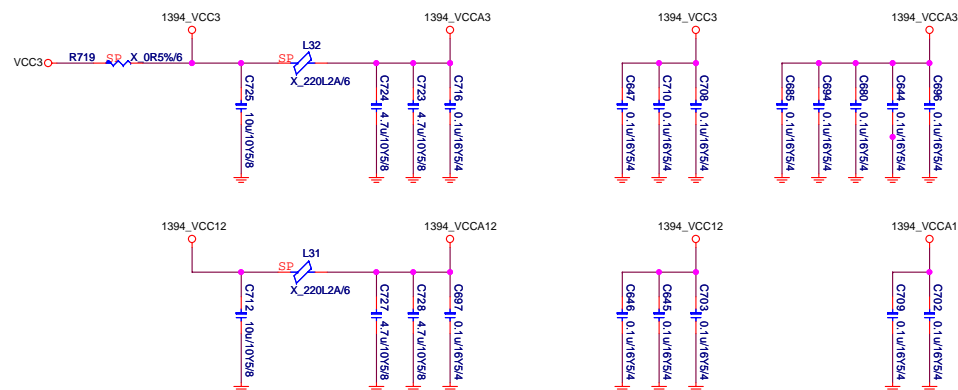


Front 1394



For Intel 1394 pinheader

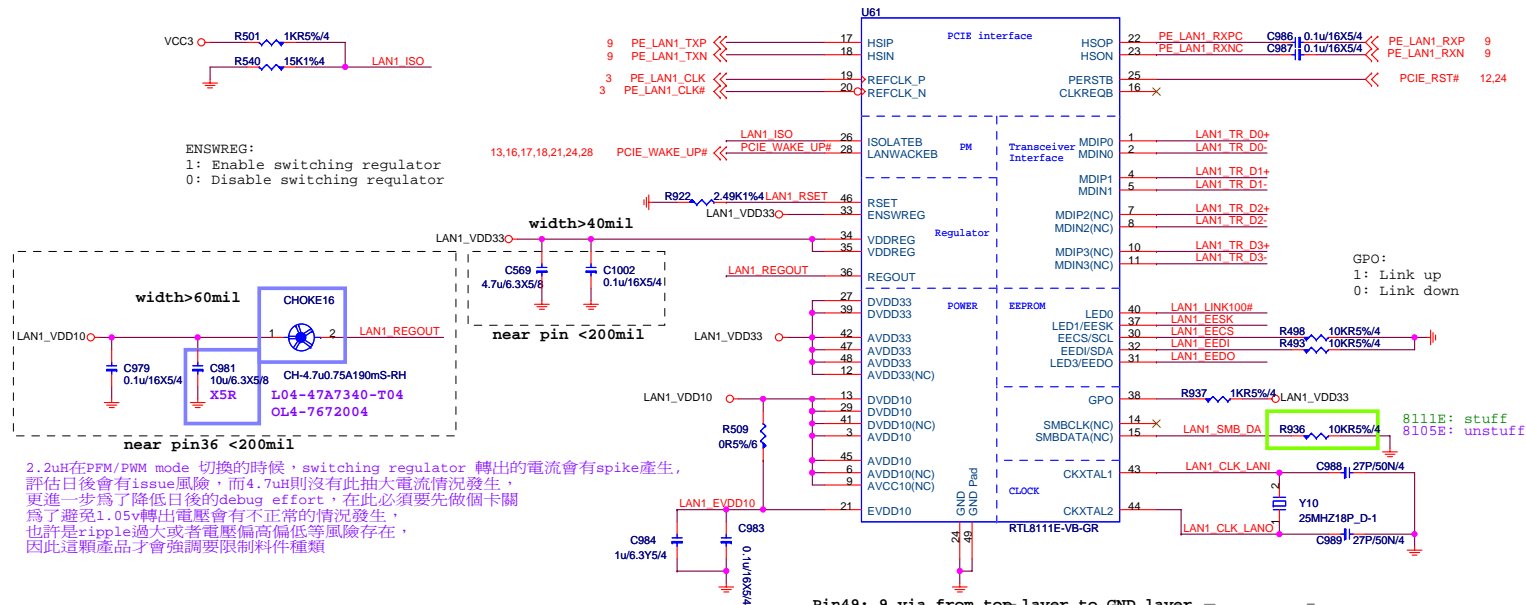
www.aitech1.ru



All 0.1u cap near to IC power pin

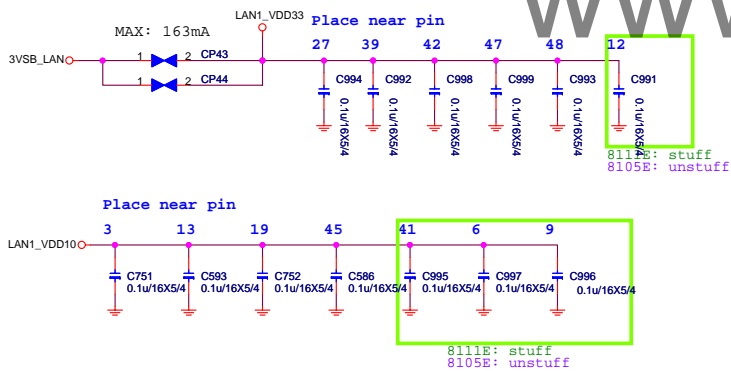
MICRO-STAR INT'L CO.,LTD			
MS-7640			
Size	Document Description	Rev	
Custom	1394 Controller - VIA VT6315N	1.4	
Date:	Tuesday, June 22, 2010	Sheet	22 of 42

RTL8105E 10/100M LAN



Pin49: 9 via from top layer to GND layer
and make the via at the center of IC.

3.3v Power on rise time : 1~100ms.

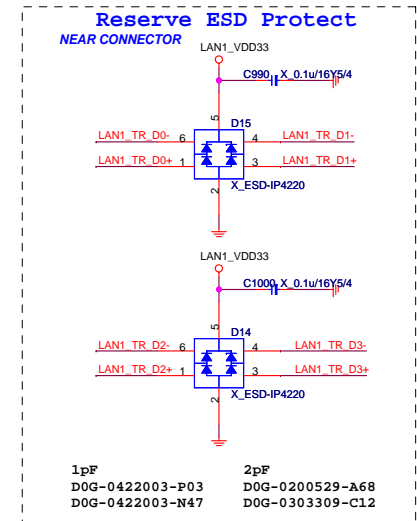
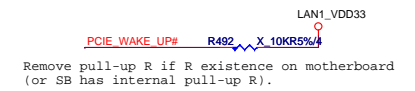
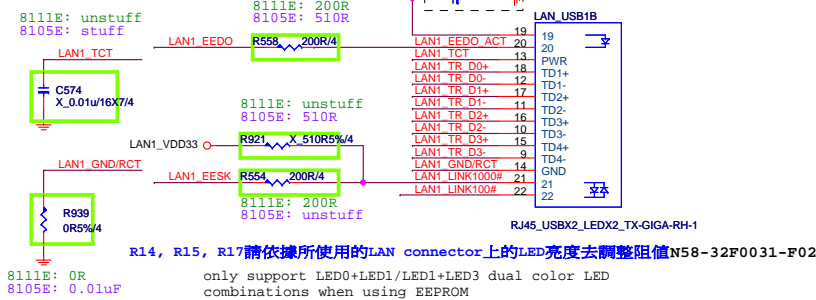





8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



Giga-Lan		10/100-Lan	
N58-22F0081-S42		N58-22F0061-S42 N58-22F0061-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	Green	22	Green

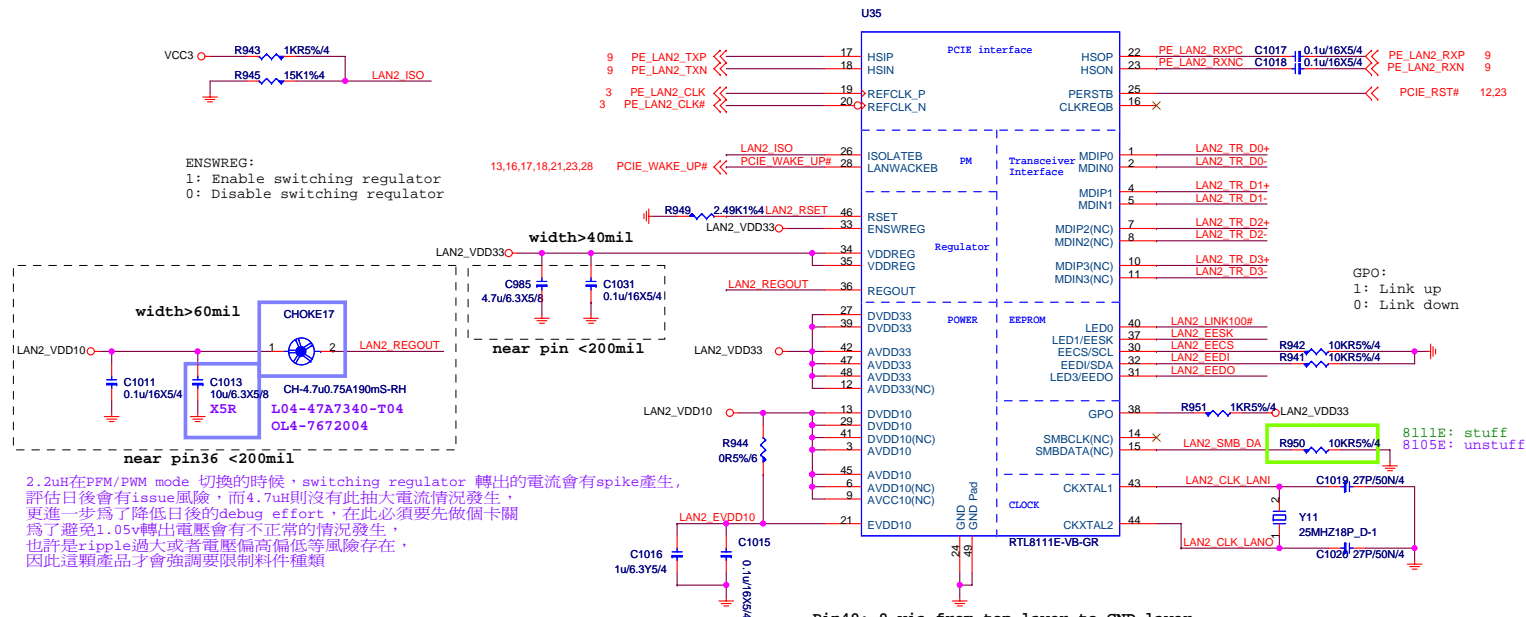


MICRO-STAR INT'L CO.,LTD

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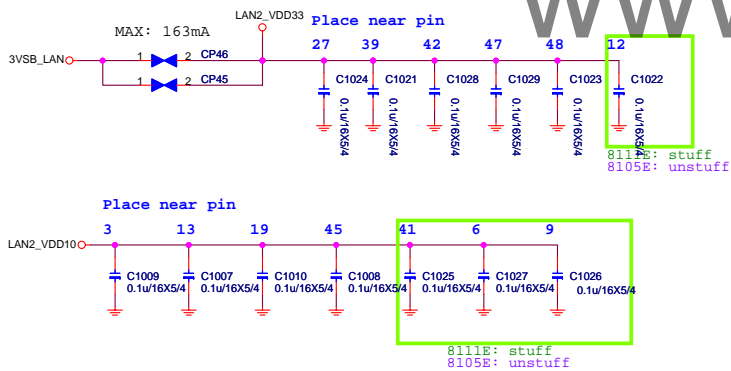
Size Custom	Document Description LANI RTL 8111E	Rev 1.4
Date: Tuesday, June 22, 2010		Sheet 23 of 42

RTL8105E 10/100M LAN



Pin49: 9 via from top layer to GND layer and make the via at the center of IC.

3.3v Power on rise time : 1~100ms.

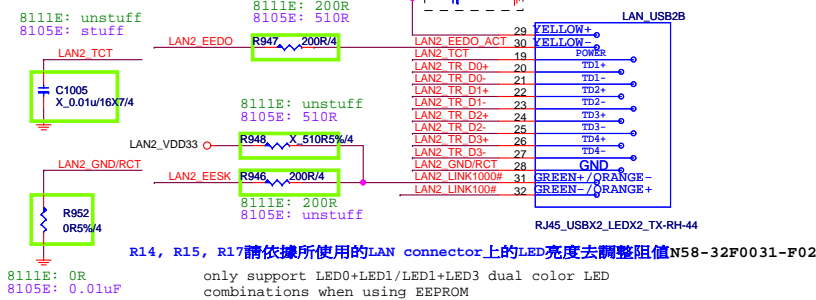


8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

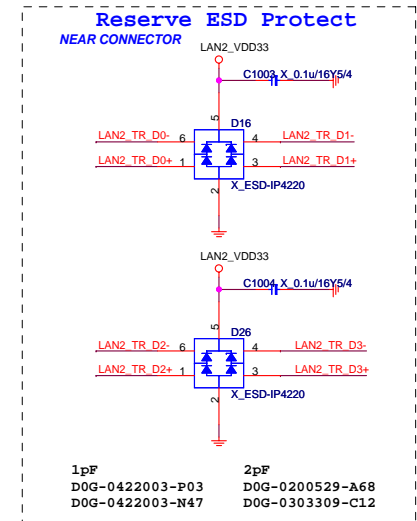
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13







LAN2_VDD33

PCIE_WAKE_UP# R940 X 10KR5%4

Remove pull-up R if R existence on motherboard (or SB has internal pull-up R).



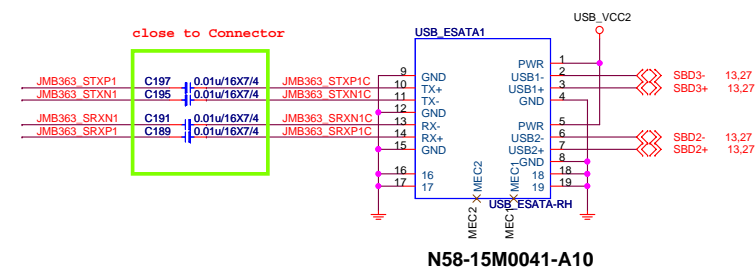
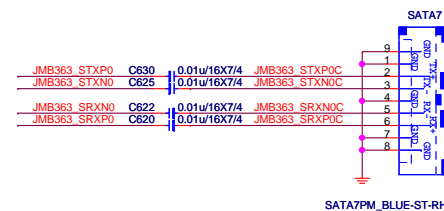
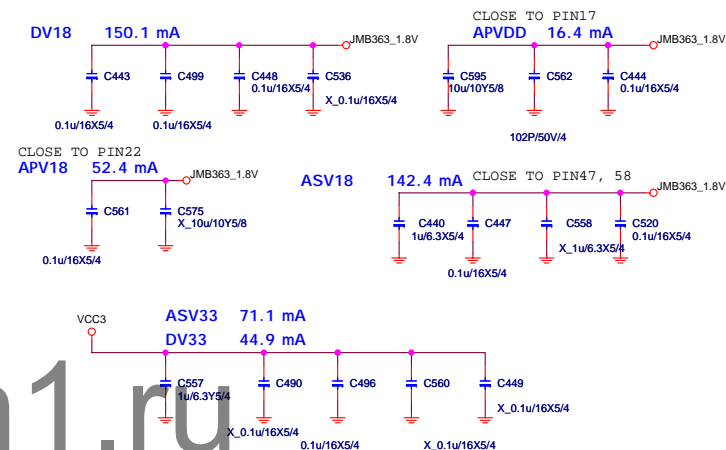
Giga-Lan		10/100-Lan	
N58-22F0081-S42		N58-22F0061-S42 N58-22F0061-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
			
22	Green	22	Green



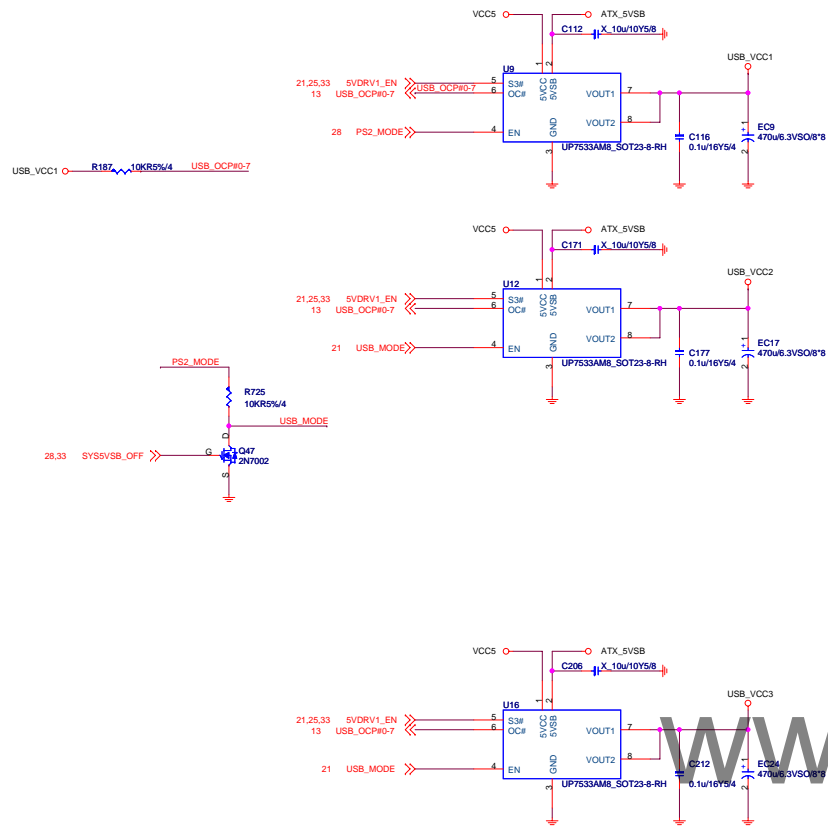
MICRO-STAR INT'L CO.,LTD

MS-7640

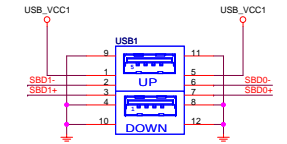
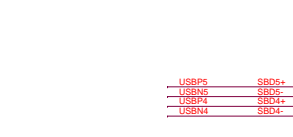
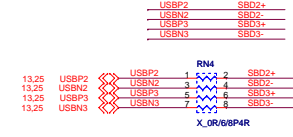
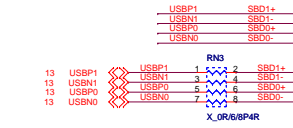
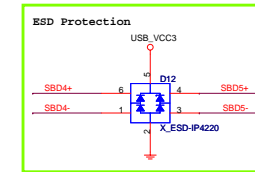
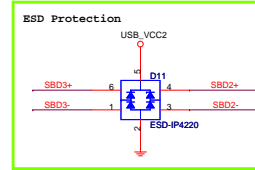
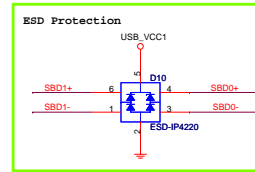
Size Custom	Document Description LAN2 RTL 8111E	Rev 1.4
Date: Tuesday, June 22, 2010		Sheet 24 of 42



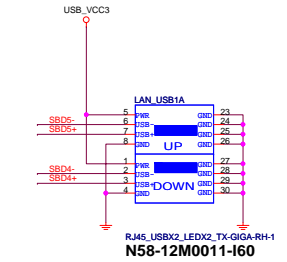
POWER CIRCUIT FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 0 - 7

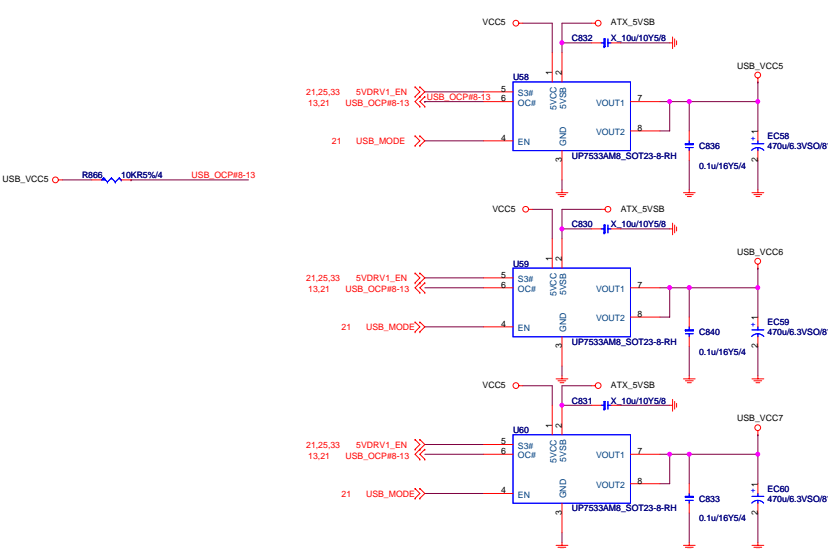


N58-12M0011-I60

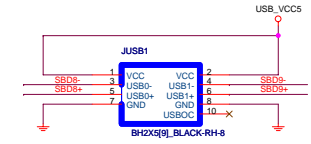
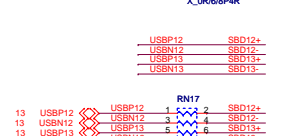
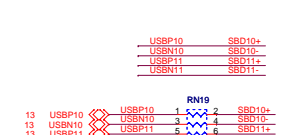
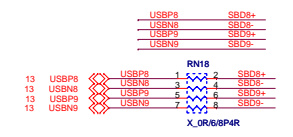
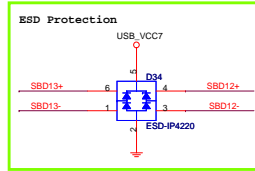
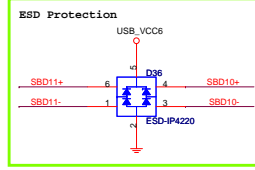
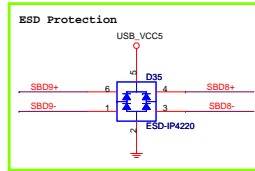


R45_USBX2_LED2_TX-GIGA-RH-1
N58-12M0011-I60

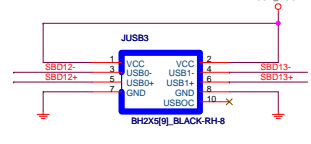
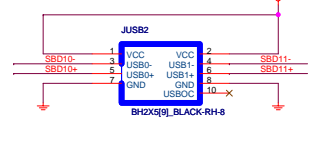
POWER CIRCUIT FOR USB PORT 8,9,10



FRONT PANEL USB CONNECTOR FOR USB PORT 8 - 11



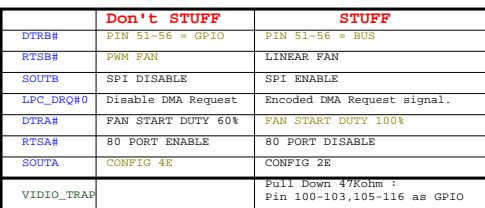
N31-2051581-H06
N32-2051371-H06(Blk, housing)



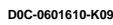
MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description	USB Connector-Front / Rear
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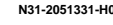
LPC SUPER I/O F71889ED



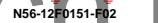
7 a



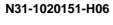
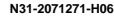
VCC5 NR1A#



F71889EF EUP Function



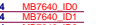
Chassis Intrusion



The best voltage input level is about 1V.

VCOR2 R745...10KR1%4 VCore_SIO





2	1	0	ROM TYPE
0	0	0	V1.1 ALC889+BIOS FAN PATCH
0	0	1	V1.2 MCU+ALC889
0	1	0	V1.3 ALC892
0	1	1	V1.1 ALC889
1	0	0	V1.4 ALC892
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



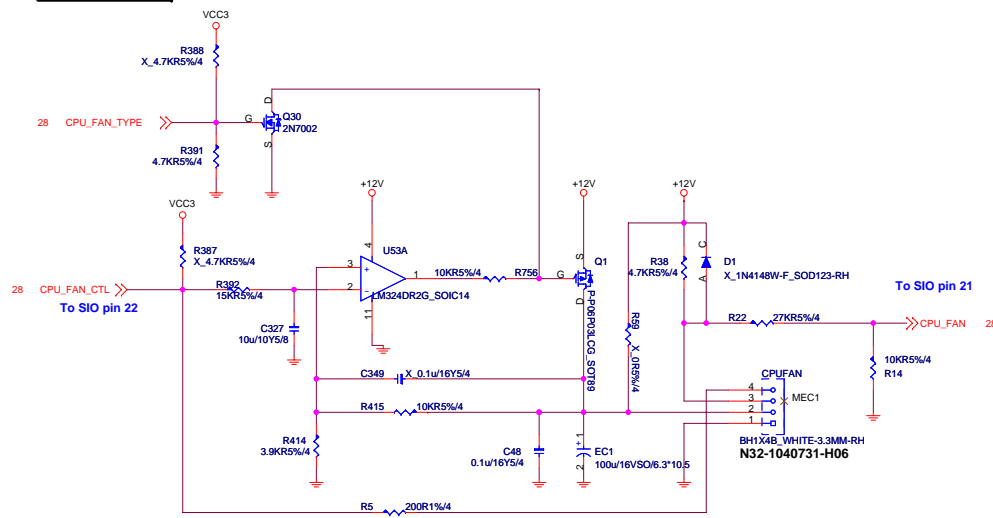
MICRO-STAR INT'L CO.,LTD

MS-7640

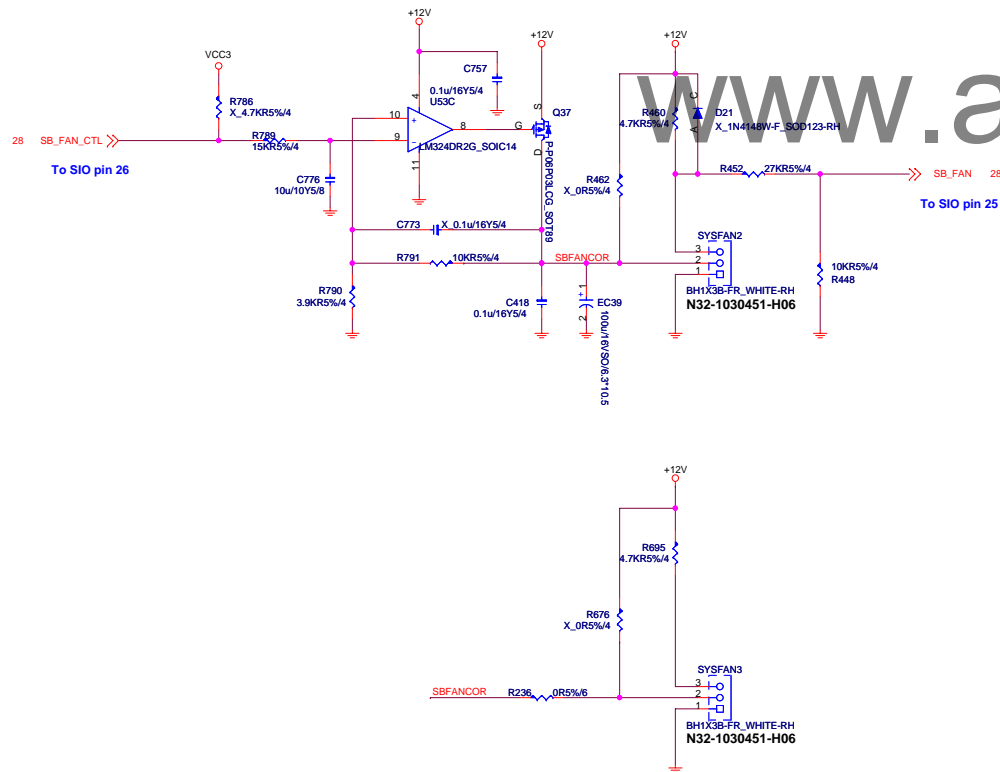
Document Description	Rev
SIO - F71889F/ FDD/ KBMS	1.4

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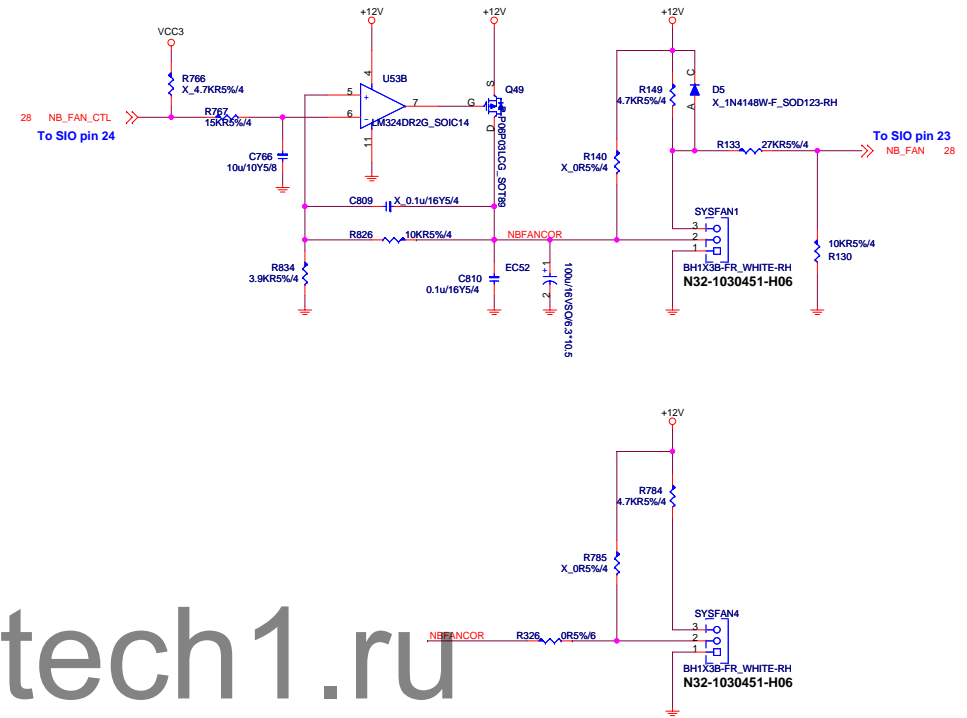
CPU FAN



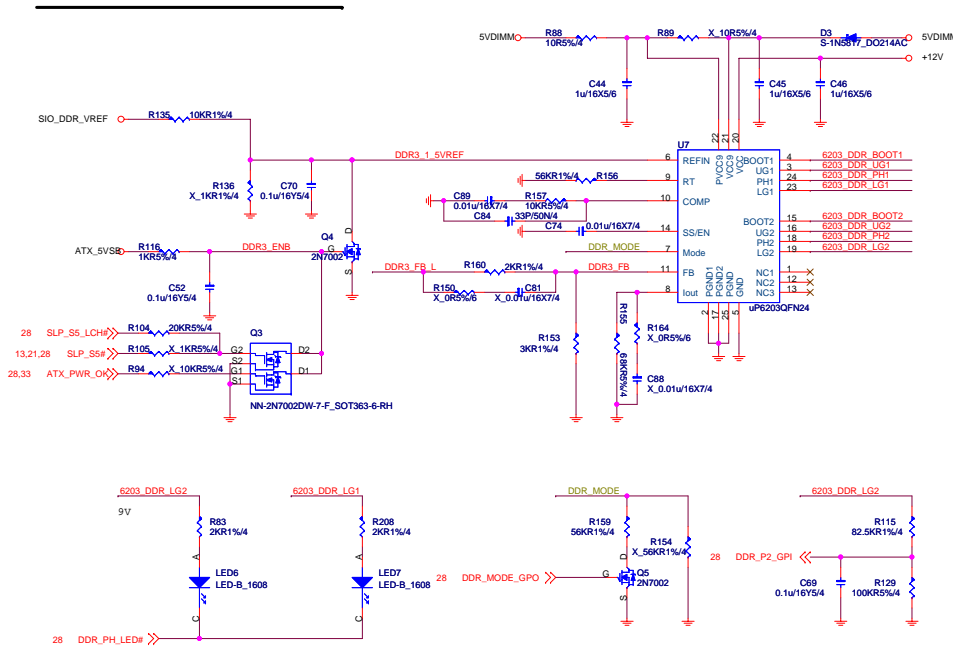
SB FAN



NB FAN

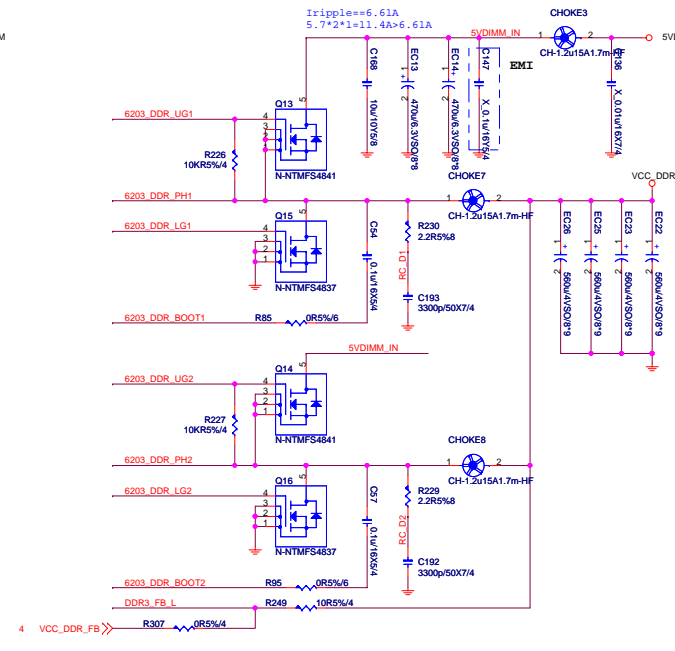


DDR III 1.5V POWER



$$V_{out} = 0.9 \left[\frac{R184+R176}{R176} \right] / R176 = 1.5 \text{ Volt}$$

$$V_{out} = 0.9 \left[\frac{2k+3k}{3k} \right] / 3k = 1.5 \text{ Volt}$$



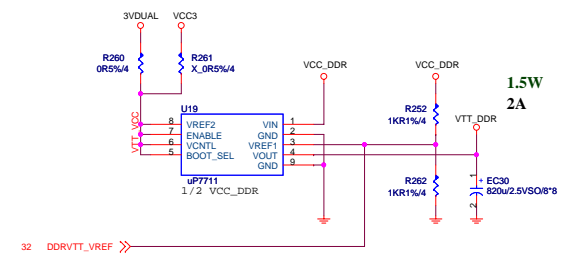
8.25A
80%, 41.25W

20+2=22A
33W

$$1.8A \cdot 6 + 0.2075A \cdot 6 + 6A = 6A + 10.8A + 1.245A = 18.045A$$

DDR VTT Power

To CPU Copper trace width > 250mils, Fill island behind DIMM > 400mils. $0.2075A \cdot 6 = 1.245A$



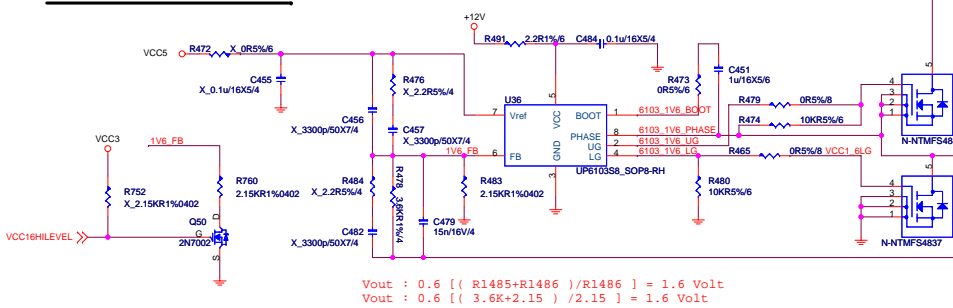
1.5W
2A

SYSTEM 1.6V POWER

80%, 31.85W

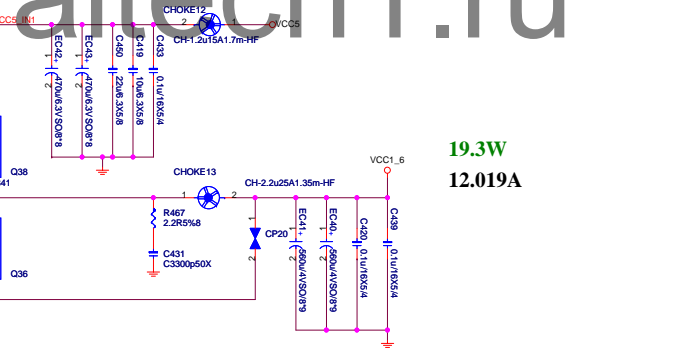
6.3A

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$$V_{out} = 0.6 \left[\frac{R1485+R1486}{R1486} \right] / R1486 = 1.6 \text{ Volt}$$

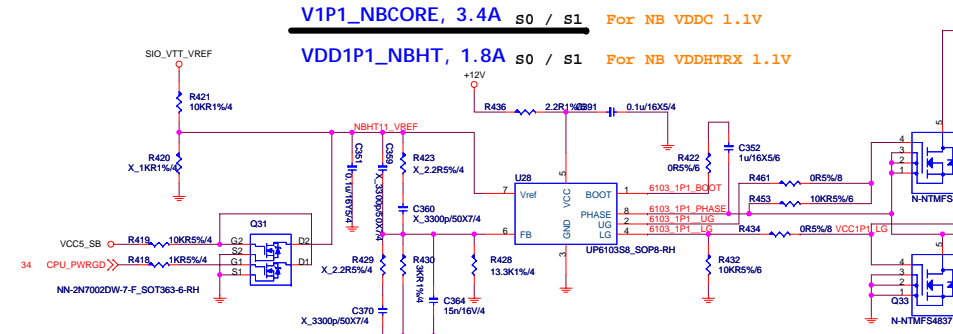
$$V_{out} = 0.6 \left[\frac{3.6K+2.15}{2.15} \right] / 2.15 = 1.6 \text{ Volt}$$



19.3W
12.019A

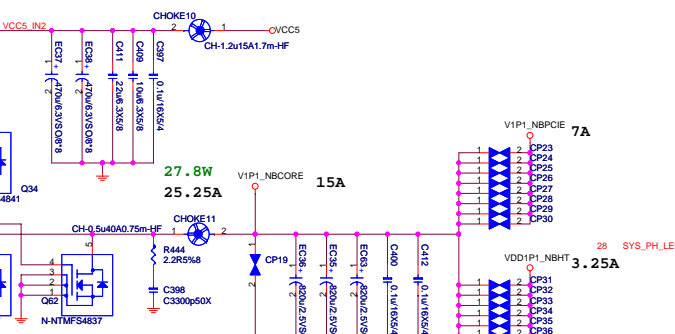
VCC1_6 change to 2.12V

V1P1_NBCORE, 3.4A S0 / S1 For NB VDDC 1.1V
VDD1P1_NBHT, 1.8A S0 / S1 For NB VDDHTRX 1.1V



$$V_{out} = 0.9 \left[\frac{R72+R1487}{R1487} \right] / R1487 = 1.1 \text{ Volt}$$

$$V_{out} = 0.9 \left[\frac{3K+13.3K}{13.3K} \right] / 13.3K = 1.1 \text{ Volt}$$



27.8W
25.25A

7A

15A

3.25A



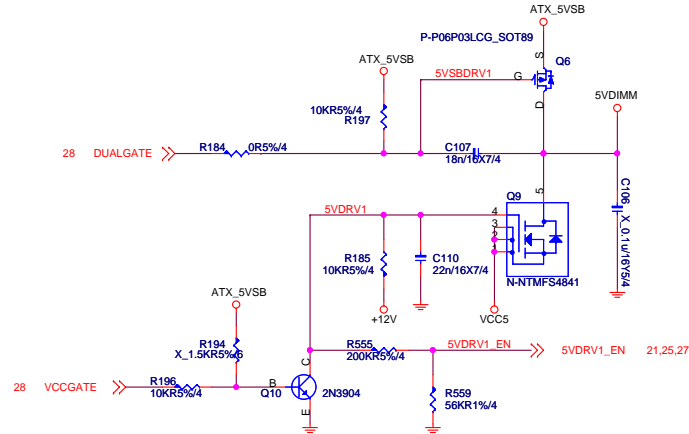
MICRO-STAR INT'L CO., LTD

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5VDIMM FOR DDR

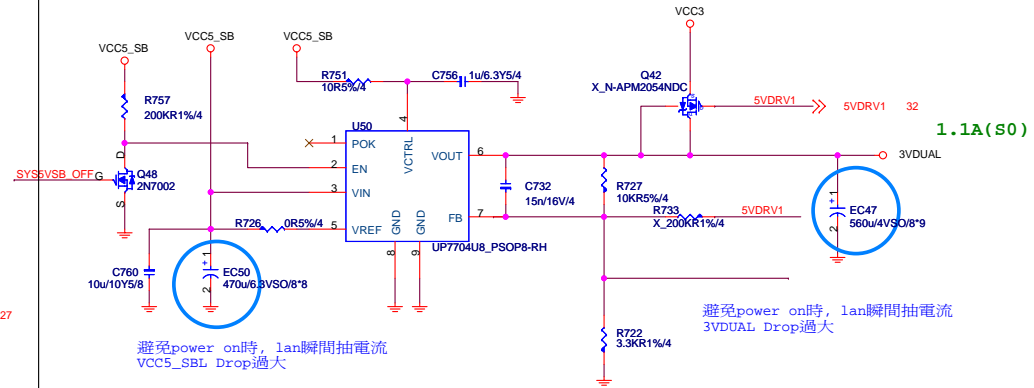
H:Support S0/S3/S5
L:Support S0/S3



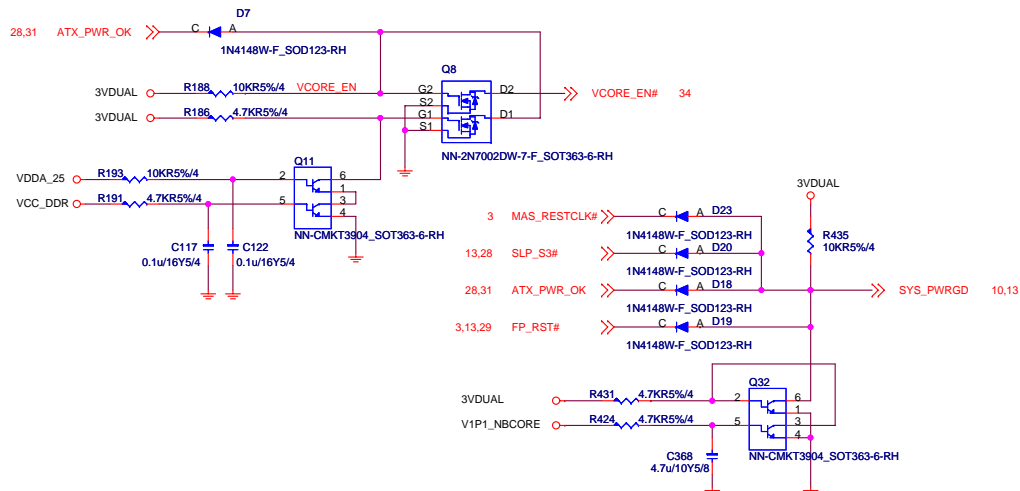
3VDUAL, 1.017A

S0 - S5

For SB USB 1.2V, 310mA
For SB 3VDUAL 3.3V, 712mA



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5VSB Power Switch

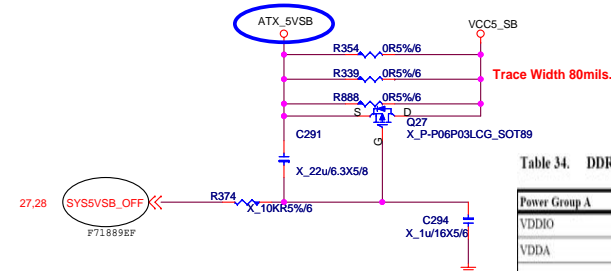
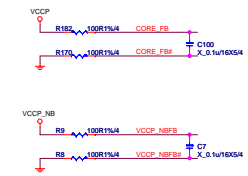
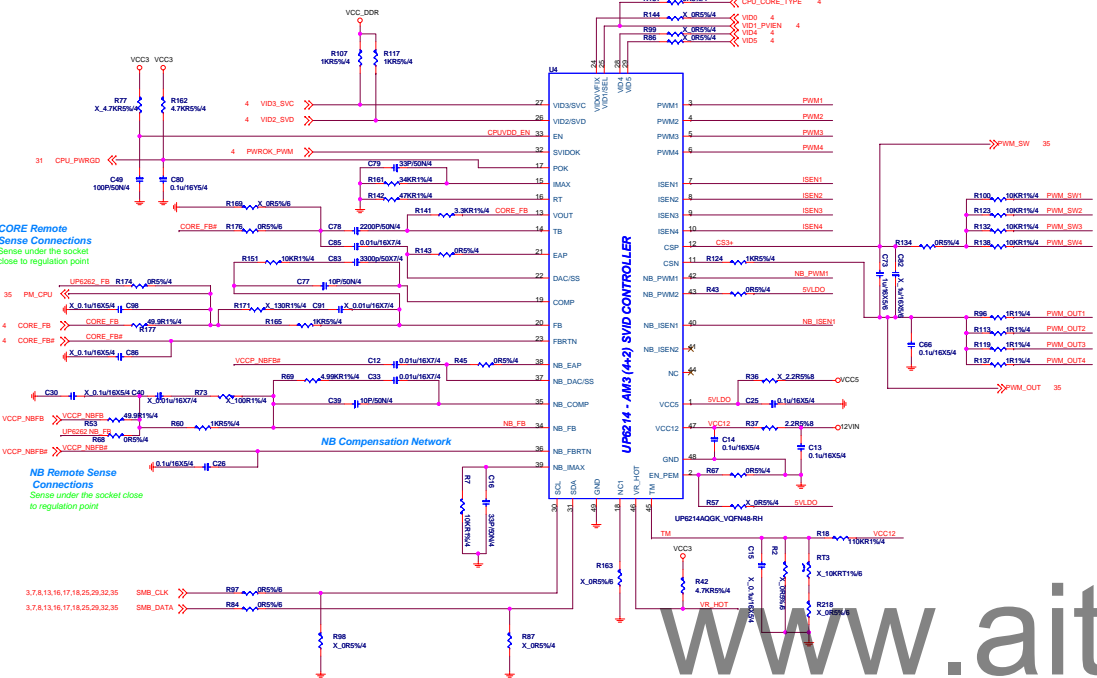


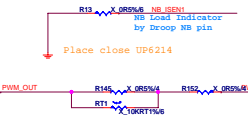
Table 34. DDR3 Power Sequencing Group Definitions

Power Group A		Power Group B	
VDDIO		VDD	
VDDA		VDDNB	
		VLDI	
		VDDR	
MICRO-STAR INT'L CO.,LTD			
MS-7640			
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Custom	ACPI Controller - UPI	1.4	
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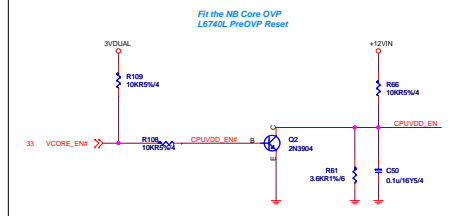
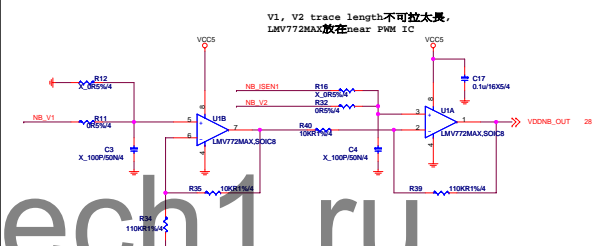
UPI up6214+Dr-MOS(R2J20604NP)



Place close UP6214



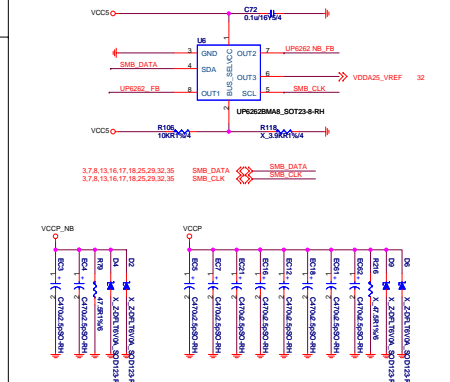
POWER WATTAGE MONITOR



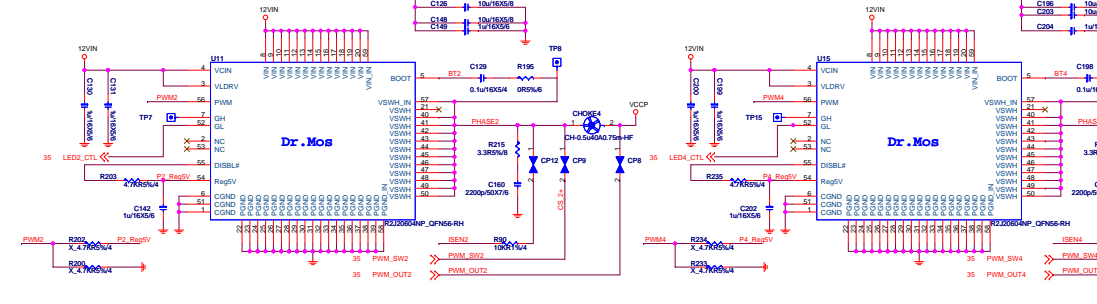
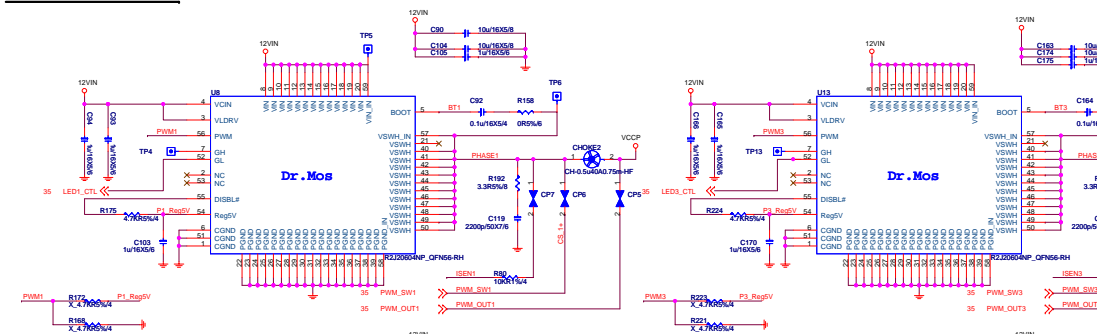
ADDRESS	0x6A	0x6B	0x6C	0x6D	0x6E
RH (KOhm)	OPEN	3.9	3	2.2	1.3
RL (KOhm)	10	1.3	2.3	3	3.9
BUS_SEL	0%	25%	40%	60%	75%

up6262不上件, R1355.R1444 不上件

100 Vcc5
0 x 60 : RH = 10K, RL = open



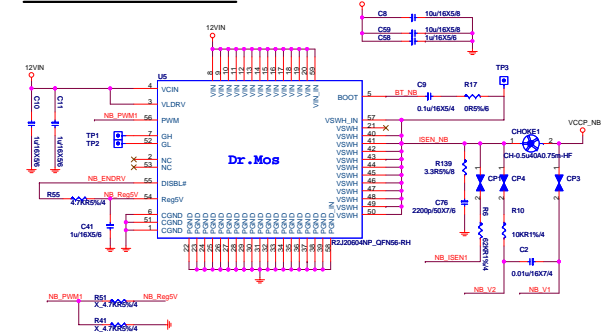
CPU_VDD_RUN



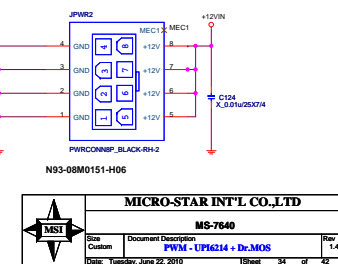
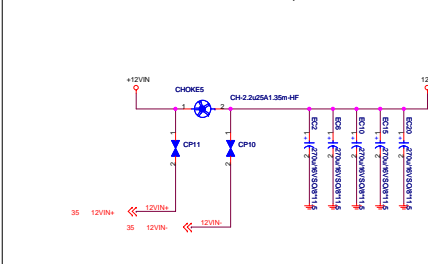
EMI



CPU_VDDNB_RUN

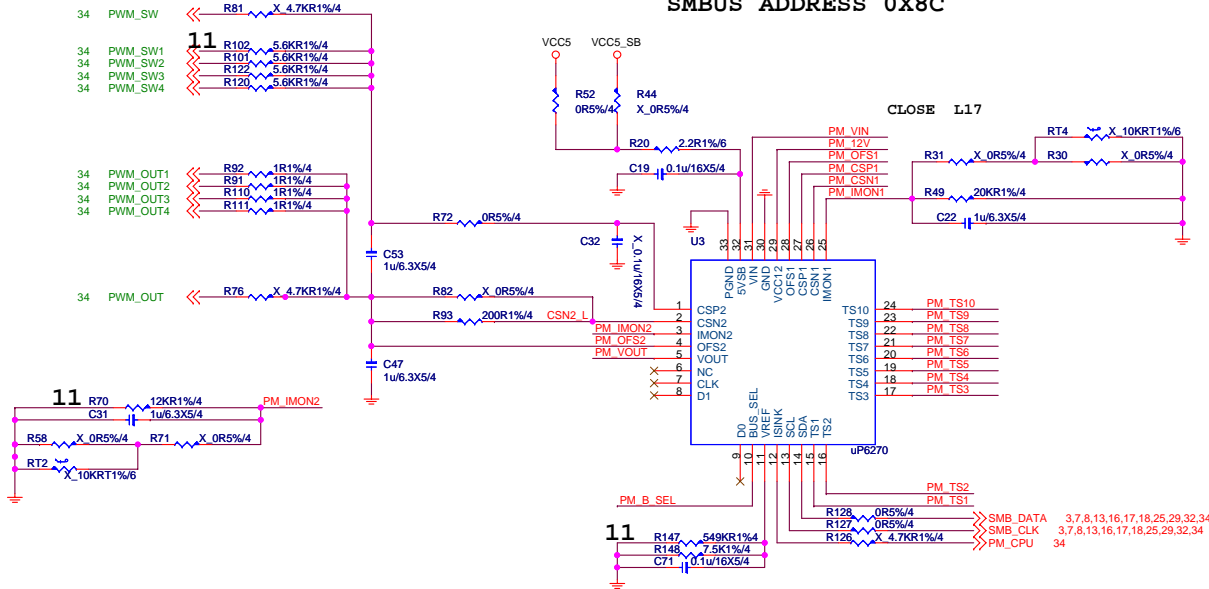


ATX Power Connector (2x4)



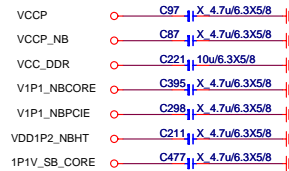
POWER METER

SMBUS ADDRESS 0X8C

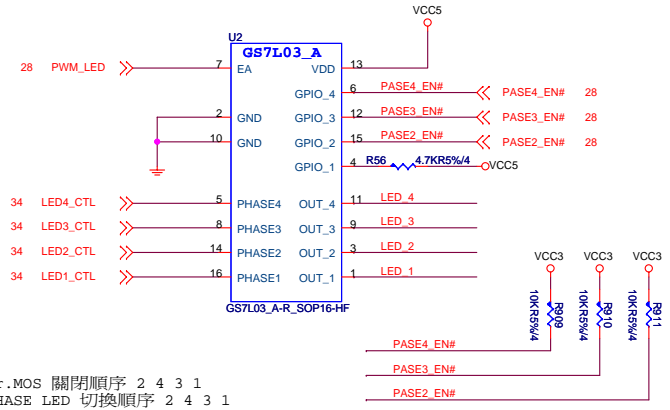


電壓測點

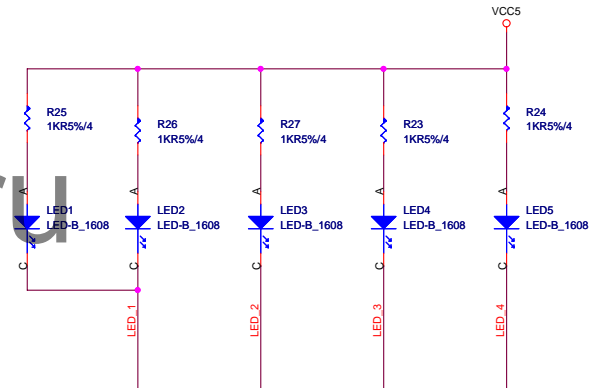
Voltage TEST POINTS



PWM LED CONTROL



Dr.MOS 關閉順序 2 4 3 1
PHASE LED 切換順序 2 4 3 1



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LED shine:S0 ~ S5

TOUCH_PAD

POWER1

X_PAD

LED shine:S0

TOUCH_PAD

Reset1

X_PAD

R849
X_1M/4

R850
1M/4

ATX_5VSB

R856
22K1%/4

C821
0.01uF/16X7/4

R859
22K/4/1

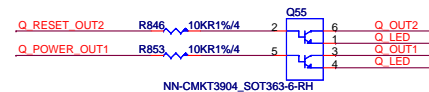
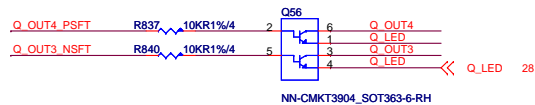
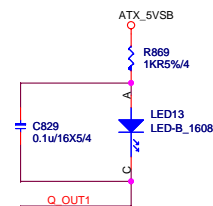
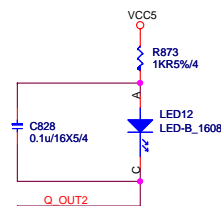
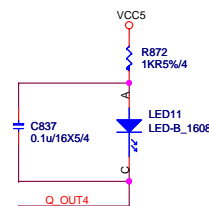
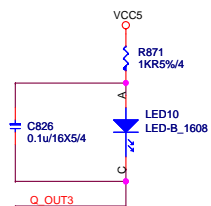
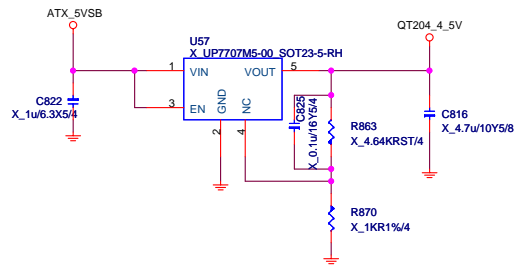
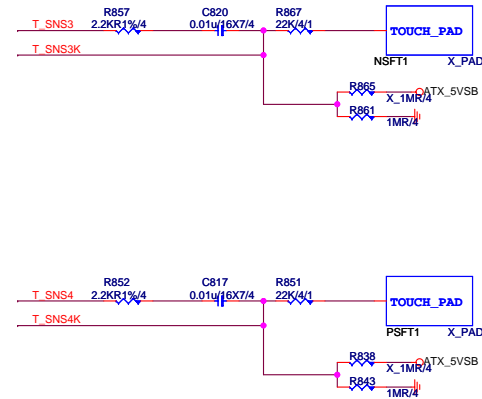
T SNS3

T SNS3K

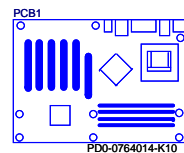
T SNS4

T SNS4K

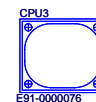
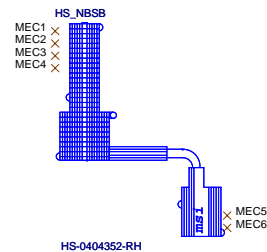
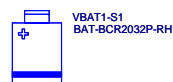
Q_POWER_OUT1	>>>	Q_POWER_OUT1	29
Q_RESET_OUT2	>>>	Q_RESET_OUT2	29
Q_OUT3_NSFT	>>>	Q_OUT3_NSFT	3
Q_OUT4_PSFT	>>>	Q_OUT4_PSFT	3



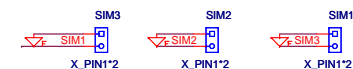
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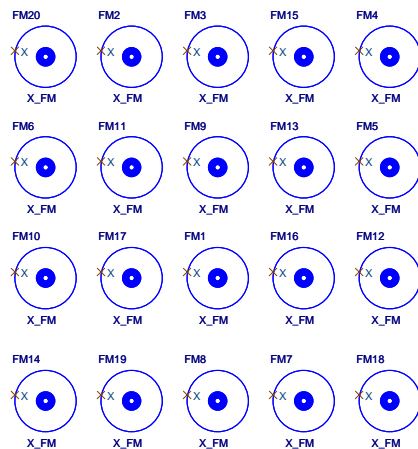
PD0-0764014-K10



Simulation



Optics Orientation Holes



Mounting Holes

